

ISO 9001:2015 Certified | DST-FIST Supported Institution Recognized under Section 2(f) & 12(B) of the UGC Act, 1956 Vannarpettai, Tirunelveli - 627003, Tamil Nadu

# M.E. – VLSI Design

## R2019-Curriculum and Syllabi 2021 – PG CHOICE BASED CREDIT SYSTEM AND OBE

## VISION OF THE DEPARTMENT

To develop Electronics and Communication Engineers by permeating with proficient morals, to be recognized as an adroit engineer worldwide and to strive endlessly for excellence to meet the confronts of our modern society by equipping them with changing technologies, professionalism, creativity research, employability, analytical, practical skills and to excel as a successful entrepreneur.

## **MISSION OF THE DEPARTMENT**

- To provide excellence through effective and qualitative teaching- learning process that equips the students with adequate knowledge and to transform the students' lives by nurturing the human values to serve as a precious resource for Electronics and Communication Engineering and nation.
- To enhance the problem solving and lifelong learning skills that will enable by edifying the students to pursue higher studies and career in research.
- To create students with effective communication skills, the abilities to lead ethical values in order to fulfill the social needs

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## FRANCIS XAVIER ENGINEERING COLLEGE, TIRUNELVELI DEPARTMENT OF ELECTRONICIS AND COMMUNICATION ENGINEERING 103 G2 Bye Pass Road, Vannarpettai, Tirunelveli, Tamilnadu – 627003 Phone : 0462 – 2502283, 2502157, Fax: 0462 – 2501007 Email :principal@francisxavier.ac.in, Website : www.francisxavier.ac.in

#### PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

**PEO 1 – Core Competence:** To demonstrate core competence in mathematics, basic sciences and engineering concepts, that apply to VLSI Design engineering knowledge and/or also to pursue advanced study or research.

**PEO 2 – Design and Analysis:** To demonstrate good skills to comprehend VLSI Design engineering trade-offs, forecast, analyse, design, and synthesize data and technical concepts to create novel solutions for real life problems.

**PEO 3 – Develop multi skills & Professionalism:** To have a successful career by meeting the demand driven needs of VLSI based industries/ profession, with multi-disciplinary projects, adhering to ethical standards with social responsibility.

#### PROGRAMME SPECIFIC OUTCOMES (PSOs)

**PSO 1:** Design, Implement and Test Embedded and VLSI systems using state of the art components and software tools

**PSO 2:** Design and develop the signal processing and communication systems for the real time application.

#### PROGRAM OUTCOMES (POs)

#### **Engineering Graduates will be able to:**

**1. Engineering Knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

2. **Problem Analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

**3. Design/Development of Solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

**4. Conduct Investigations of Complex Problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

**5.** Modern Tool Usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

6. The Engineer and Society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

7. Environment and Sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

**8.** Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

**9.** Individual and Team Work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

**10. Communication**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

**11. Project Management and Finance**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

**12. Life-Long Learning**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

## Mapping with PO Vs PEO, PSO

PO	PEO1	PEO2	PEO3	<b>PSO1</b>	PSO2
1		Н		Н	
2		Н		М	
3		L	Н		
4	Н	L			Н
5				Н	
6			L		
7					Н
8	L				Н
9	L			М	
10	М			М	
11	М				Н
12	L	М	Н		

Contribution L: Low / Reasonable M: Medium / Significant H:High / Strong

## FRANCIS XAVIER ENGINEERING COLLEGE M.E VLSI DESIGN REGULATIONS 2019 Choice Based Credit System and Outcome Based Education

#### **CREDITS PER SEMESTER** TOTAL CREDITS S. No CATEGORY IN % CREDIT Ι II III IV 3 1 ES 3 4% 30 2 PC 14 9 7 41.8% 18 3 PE 6 12 25% 4 7 EEC 2 12 21 29.2% TOTAL 23 23 14 12 72 100%

#### SUMMARY OF CREDIT DISTRIBUTION

#### Minimum Number of Credits to be Acquired: 72

- ES Engineering Sciences
- PC Professional Core
- PE Professional Elective
- EEC Employability Enhancement Course

#### FRANCIS XAVIER ENGINEERING COLLEGE

#### M.E VLSI DESIGN REGULATIONS 2019

#### **Choice Based Credit System and Outcome Based Education**

#### I – IV Semesters Curricula and Syllabi 2021

#### **SEMESTER I**

S.No.	Course	Course	Category	Contact	L	Т	Р	С
Theor	v Courses			Perious				
1	21MA1255	Advanced Mathematics for VLSI	ES	3	2	1	0	3
2	21VL1601	CMOS VLSI Design	PC	3	3	0	0	3
3	21VL1602	Analog and Digital IC Design	PC	3	3	0	0	3
4	21VL1603	Advanced Digital System Design	PC	3	3	0	0	3
5		Professional Elective I	PE	3	3	0	0	3
6		Professional Elective II	PE	3	3	0	0	3
7	21CS1605	Research Methodology for Engineers	PC	3	3	0	0	3
Practi	cal Courses							
1	21VL1611	Advanced Digital System Design Laboratory	PC	4	0	0	4	2
			Total	25	20	1	4	23

#### **SEMESTER II**

	Code	Course	Category	Contact Periods	L	Т	Р	С
Theory	Courses							
1	21VL2601	Low Power VLSI Design	PC	3	3	0	0	3
2		Professional Elective III	PE	3	3	0	0	3
3		Professional Elective IV	PE	3	3	0	0	3
4		Professional Elective V	PE	3	3	0	0	3
5		Professional Elective VI	PE	3	3	0	0	3
Theory	cum Practi	cal Courses						
1	21VL2602	IC Design for Communications	PC	5	3	0	2	4
Practica	al Courses							
1	21VL2611	Analog and Digital IC Design Laboratory	PC	4	0	0	4	2
2	21VL2911	Advanced Design and Analysis Laboratory	EEC	4	0	0	4	2
			Total	28	18	0	10	23

#### SEMESTER III

S.No.	Course Code	Course	Category	Contact Periods	L	Т	Р	С
Theory	cum Practic	al Courses						
1	21VL3601	Physical Design of Integrated Circuits	PC	5	3	0	2	4
2	21VL3602	ASIC Design	PC	3	3	0	0	3
Practic								
1	21VL3911	Term Paper Writing	EEC	2	0	0	2	1
2	21VL3912	Dissertation I	EEC	12	0	0	12	6
			Total	22	6	0	16	14

#### **SEMESTER IV**

S.No.	Course Code	Course	Category	Contact Periods	L	Т	Р	С
Practic	al Courses							
1	21VL4911	Dissertation II	EEC	24	0	0	24	12
			Total	24	0	0	24	12

### Minimum Number of Credits to be Acquired: 72

L - Lecture T-Tutorial	P- Practical	H- Hours	C- Credit	
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## List of Engineering Science Courses

S.No	Course Code	Course Name	Category	Contact Periods	L	Т	Р	C
Theory	<b>Courses</b>							
1	21MA1255	Advanced Mathematics for VLSI	ES	3	2	1	0	3

#### List of Employability Enhancement Courses

S.No	Course Code	Course Name	Category	Contact Periods	L	Т	Р	С
Practic	al Courses							
1	21VL2911	Design and Analysis Laboratory	EEC	4	0	0	4	2
2	21VL3911	Term Paper Writing	EEC	2	0	0	2	1
3	21VL3912	Dissertation I	EEC	12	0	0	12	6
4	21VL4911	Dissertation II	EEC	24	0	0	24	12

#### List of Professional Electives Courses

S.No.	Cada Na	Course	Compositor	т	т	р	C	Stream/
	Code No.	Course	Semester	L	1	P	C	Domain
Profes	sional Elective	Ι						
1	21VL1701	Nano-Electronic Devices and Materials	Ι	3	0	0	3	Nano Technology
2	21VL1702	MEMS and NEMS	Ι	3	0	0	3	Nano Technology
3	21VL1703	Flexible Electronics	Ι	3	0	0	3	VLSI
4	21VL1704	Reliability of Devices and Circuits	Ι	3	0	0	3	Electronic Devices
Profes	sional Elective	e II						
1	21VL1705	Graph Theory and Algorithms for CAD	Ι	3	0	0	3	CAD
2	21VL1706	Communication Buses and Interfaces	Ι	3	0	0	3	Communication
3	21VL1707	Mixed Signal Design	Ι	3	0	0	3	VLSI
4	21VL1708	VLSI Architectural Design and Implementation	Ι	3	0	0	3	VLSI
Profes	sional Elective	e III						
1	21VL2701	VLSI Signal Processing	II	3	0	0	3	VLSI
2	21VL2702	Scripting Languages for VLSI	II	3	0	0	3	VLSI
3	21VL2703	Advanced Memory Technologies	II	3	0	0	3	VLSI
4	21VL2704	System on Chip Design	II	3	0	0	3	VLSI

S.No.	Cada Na	Course	Comostor	т	т	р	C	Stream/
	Code No.	Course	Semester	L	I	r	C	Domain
Profes	sional Elective	e IV				1		
1	21VL2705	VLSI Test and Testability	II	3	0	0	3	VLSI
2	21VL2706	VLSI Digital Design Verification	II	3	0	0	3	VLSI
3	21VL2707	Modern Computer Architecture	II	3	0	0	3	Computer Science
4	21VL2708	Electronic Design Automation	II	3	0	0	3	Electronics
Profes	sional Elective	e V		•	•	•		
1	21VL2709	Modelling and Simulation of Solid-State Circuits	II	3	0	0	3	VLSI
2	21VL2710	Internet of Things	II	3	0	0	3	Embedded
3	21VL2711	Hardware/Software Co-design	II	3	0	0	3	Embedded
4	21VL2712	3D IC Design and Modeling	II	3	0	0	3	VLSI
Profes	sional Elective	e VI			•			
1	21VL2713	Embedded System and RTOS	II	3	0	0	3	Embedded
2	21VL2714	VLSI for Biomedical Applications	II	3	0	0	3	VLSI
3	21VL2715	Advanced Microprocessors and Architectures	II	3	0	0	3	Embedded

#### **SEMESTER I**

S.No.	Course Code	Course	Category	Contact Periods	L	Т	Р	C
Theor	y Courses	-	•			-		
1	21MA1255	Advanced Mathematics for VLSI	ES	3	2	1	0	3
2	21VL1601	CMOS VLSI Design	PC	3	3	0	0	3
3	21VL1602	Analog and Digital IC Design	PC	3	3	0	0	3
4	21VL1603	Advanced Digital System Design	PC	3	3	0	0	3
5		Professional Elective I	PE	3	3	0	0	3
6		Professional Elective II	PE	3	3	0	0	3
7	21CS1605	Research Methodology for Engineers	PC	3	3	0	0	3
Practi	cal Courses							
1	21VL1611	Advanced Digital System Design	PC	4	0	0	4	2
		Laboratory	Total	25	20	1	4	23
				L				
211	MA1255	ADVANCED MATHEMATICS	FOR VLSI		L	Т	Р	С
				2	2	1	0	3
Prer	equisites for	the course						
•	The pre-req mathematic	uisite knowledge required by the Students s.	to study this	s Course is	basio	e kno	wled	ge in
Obje	ctives							
1.	To demonst	trate various analytical skills in applied ma	thematics an	d extensive	e exp	erier	ice wi	th
2	the statistic	s of problem solving and logical thinking a	applicable in	electronics	engi	ineer	ing.	1
Ζ.	tools	, formulate, abstract and solve problems in	electrical en	gineering i	ising	mat	nemai	ical
3.	To discuss	the linear algebra and linear programming						
4.	To know tł	ne importance of the probability and ran	dom variab	les				
5.	To analyse	the dynamic programming and queuein	g Models					
U	INIT I	LINEAR ALGEBRA				Ģ	9	
Vecto	or Spaces-Nor	ms-Inner Products-Eigen Values using tra	nsformation-	QR Factor	izati	on-G	enera	lized
Eigen Squar	Vectors-Car e approximat	nonical Forms-Single value decomposition	on and Appl	ications-Ps	seudo	o inv	erse-l	Least
U	NIT II	LINEAR PROGRAMMI	NG			Ģ	9	
Form	ulation-Graph	nical Solution-Simplex Method-Big M M	ethod-Transp	portation P	roble	m-A	ssign	ment
mode	ls							
U		PROBABILITY AND RANDOM	VARIABLE	S		(	9	
<u> </u>								

UNIT IV	DY	NAMIC PROGRAMMING		9
Dynamic progr Dynamic progr	amming- Principle of amming- Problem of c	optimality- Forward and backward rec limensionality	cursion-	Applications of
UNIT V		QUEUEING MODELS		9
Poisson proces analysis	s- Markovian queues	- Single and Multi –server models-	Little's	formula Steady sta
		Total Pe	eriods	45
Suggestive As	sessment Methods			
Continuous A (30 Mai	ssessment Test	formative Assessment Test (10 Marks)	End Sei (60 Ma	mester Exams rks)
1. Descrip	tion Questions	1. Assignment	1.	Description
<b>2.</b> Format	ive Multiple Choice	2. Online Quizzes	(	Questions
Questic	ons	<b>3.</b> Problem Solving	<b>2.</b> ]	Formative Multiple
Outcomes		Activities	(	Lnoice Questions
Unon comple	tion of the course t	he students will be able to:		
CO255. 1	Concepts of fuzzy se	ts, knowledge representation using fuz	zzy rules	s, fuzzy logic,
	fuzzy prepositions an	d fuzzy quantifiers and applications o	of fuzzy 1	logic.
CO255. 2	Apply various metho	ds in matrix theory to solve system of	linear e	quations.
CO255. 3	Computation of prob	ability and moments, standard distribu	itions of	discrete and
	continuous random v	ariables and functions of a random va	riable.	
CO255. 4	Conceptualize the price computational proces	inciple of optimality and sub-optimiza lure of dynamic programming	tion, for	mulation and
CO255. 5	Exposing the basic cl analyzing queuing m	haracteristic features of a queuing syst odels.	tem and	acquire skills in
Text Books				
1. George J. Kl	ir and Yuan, B., Fuzzy	sets and fuzzy logic, Theory and app	lications	s, Prentice Hall of
India Pvt. Lt	d., 1997.			
2. Moon, T.K.,	Sterling, W.C., Mathe	matical methods and algorithms for si	ignal pro	cessing, Pearson
Education, 2	000			
Reference Bo	oks			
1. Richard Johr	nson, Miller & Freund	's Probability and Statistics for Engine	eers, 7th	Edition, Prentice –
Hall of India	, Private Ltd., New De	elhi (2007).		
2.Taha, H.A., C	Operations Research, A	An introduction, 7thedition, Pearson ec	lucation	editions, Asia, New
Delhi, 2002.				
3. Donald Gros	s and Carl M. Harris.	Fundamentals of Queuing theory, 2nd	edition.	John Wiley and
	,-		,	

21VL1601		CMOS VLSI DESIGN		L	Т	Р	C
				3	0	0	3
Prerequisites f	or the course			3	U	U	3
The pre-re-	equisite knowledge i	required by the Students to study this	s Course	is basi	c kn	owled	ge in
Digital De	esign and Electron D	Devices.					8
	-						
Objectives							
1. To Descri	ibe basics of CMOS	digital integrated circuits					
2. To discus	s the fabrication pro-	cess in CMOS technologies.					
3. To Analy	ze Static & Dynamic	CMOS Design VLSI circuits.					
4. To Design	n and analyze digital	CMOS circuits.					
5. To Descri	ibe the memory proc	ess for VLSI circuits					
UNIT I	МО	S TRANSISTOR THEORY				9	
The MOS(FET)	Transistor, n MOS/	p MOS transistor, threshold voltage	e equation	n, bod	y eff	fect, I	Long-
Channel I-V Cha	racteristics-V Charae	cteristics,Non ideal I-V Effects, DC	Transfer (	Charac	cteris	stics- S	Static
CMOS Inverter I	DC Characteristics- H	Beta Ratio Effects- Noise Margin, CN	MOS techn	ologie	S		
UNIT II	CMOS TECHNOLO	OGIES, CIRCUIT CHARACTERIZAT	ΓION &			9	
p well / n well /	twin well process.	Lavout design rules. Stick diagram.	CMOS r	proces	s enł	nancei	ment.
propagation dela	vs. RC delay Line	. Delay estimation. Logical effort	and tran	nsistor	sizi	ng. P	ower
dissipation, Inter	connect design marg	in, Reliability, scaling of MOS circu	its			0,	
UNIT III	STATIC	& DYNAMIC CMOS DESIGN				9	
Static CMOS E	Design- Complemen	tary CMOS- Ratioed Logic (Pse	udo NM	OS, 1	DCV	'SL)-	Pass
Transistor Logic	- Transmission gate	logic - Dynamic CMOS Design, S	peed and	Power	r Dis	sipati	on of
Dynamic Logic, I	Issues in Dynamic D	esign, Cascading Dynamic Gates.					
UNIT IV	D	IGITAL CMOS DESIGN				9	
Sequencing Station	c Circuits-Static Late	ches and Registers - Dynamic Latch	es and Re	egister	s - P	ulse E	Based
Registers - Sense	Amplifier based reg	gisters -Latch vs. Register based pip	eline stru	ctures	, Syr	nchror	nizers
and Arbiters							
UNIT V		MEMORY ARRAY				9	
Semiconductor M	Iemories—An Introd	luction, The Memory Core, Memory	Peripher	al Circ	cuitry	, Mer	nory
Reliability and Y	ield, Case Studies in	Memory Design					·
		Total I	Periods		4	ł5	
Suggestive Asso	essment Methods						
Continuous Ass (30 Mark	sessment Test s)	Formative Assessment Test (10 Marks)	mester Exams urks)				
1. Descripti	on Questions	1. Assignment	1.	Description			
<b>2.</b> Formativ	e Multiple Choice	2. Online Quizzes		Questions			
Question	S	<b>3.</b> Problem Solving	Formative Multiple				
		Activities		Choice	e Qu	estior	IS

#### Outcomes

#### Upon completion of the course, the students will be able to:

- CO601. 1 Describe basics of CMOS digital integrated circuits
- CO601. 2 Discuss the fabrication process in CMOS technologies.
- CO601. 3 Analyze Static & Dynamic CMOS Design VLSI circuits.
- CO601. 4 Design and analyze digital CMOS circuits.
- CO601. 5 Describe the memory process for VLSI circuits

#### **Text Books**

- 1. CMOS VLSI Design-A Circuits and Systems Perspective, Fourth Edition, Neil H. E. Weste, David Money Harris, 2011
- 2. Digital Integrated Circuits A Design Perspective-Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic

#### **Reference Books**

- 1. Wayne Wolf, "Modern VLSI Design: System on Silicon", 3rd Edition, PHI, 2008.
- 2. Douglas A Pucknell, Kamran Eshraghian, "Basic VLSI Design", PHI, 3rd Edition, 2009.
- 3. Sung Mo Kang, Yosuf Leblebici, "CMOS Digital Integrated Circuits: Analysis and Design", Tata McGraw-Hill, 3rd Edition, 2003.

#### Web Resources

- 1. <u>http://www.cmosvlsi.com/</u>
- 2. <u>https://www.pearson.com/us/higher-education/program/Weste-CMOS-VLSI-Design-A-</u> <u>Circuits-and-Systems-Perspective-4th-Edition/PGM289886.html</u>
- 3. <u>https://onlinecourses.nptel.ac.in/noc20\_ee29/preview</u>

#### CO Vs PO Mapping and CO Vs PSO Mapping

CO	PO1	PO2	PO3	PO4	PO5	PO6	<b>PO7</b>	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	2		1												
2	2	3											2		
3	3			1										2	
4	2	2											3		
5	1		2												

#### $1 \rightarrow Low 2 \rightarrow Medium 3 \rightarrow High$

21VL1602	ANALOG AND DIGITAL IC DESIGN	L	Τ	Р	C
		3	0	0	3
Prerequisites f	or the course				

• The pre-requisite knowledge required by the Students to study this Course is basic knowledge in Electronic circuits, digital circuits and VLSI Design.

#### Objectives

1. To study MOS devices modelling and scaling
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- 2. To familiarize the design of single stage and multistage MOS amplifier.
- 3. This course deals comprehensively with all aspects of transistor level design of all the digital building blocks common to all CMOS microprocessors, DPSs, network processors, digital backend of all wireless systems etc.
- 4. The focus will be on the transistor level design and will address all important issues related to size, speed and power consumption
- 5. To analyse the sequential logic circuits

**UNIT I MOSFET METRICS** 9 Simple long channel MOSFET theory -SPICE Models -Technology trend, Need for Analog design -Sub-micron transistor theory, Short channel effects, Narrow width effect, Drain induced barrier lowering, Sub-threshold conduction, Reliability, Digital metrics, Analog metrics, Small signal parameters, Unity Gain Frequency, Miller"s approximation

#### SINGLE STAGE AND TWO STAGE AMPLIFIERS UNIT II

Single Stage Amplifiers -Common source amplifier with resistive load, diode load, constant current load, Source degeneration Source follower, Input and output impedance, Common gate amplifier -Differential Amplifiers -differential and common mode response, Input swing, gain, diode load and constant current load -Basic Two Stage Amplifier, Cut-off frequency, poles and zeros 9

9

9

UNIT III **CURRENT MIRRORS AND REFERENCE CIRCUITS** 

Cascode, Negative feedback, Wilson, Regulated cascode, Bandgap voltage reference, Constant Gm biasing, supply and temperature independent reference, curvature compensation, trimming, Effect of transistor mismatch in analog design

UNIT IV	COMBINATIONAL LOGIC CIRCUITS	9

Propagation Delays, Stick diagram, Layout diagrams, Examples of combinational logic design, Elmore"s constant, Dynamic Logic Gates, PassTransistor Logic, Power Dissipation, Low Power Design principles.

UNIT V

#### **SEQUENTIAL LOGIC CIRCUITS**

Static Latches and Registers, Dynamic Latches and Registers, Timing Issues, Pipelines, Pulse and sense amplifier based Registers, Non bistable Sequential Circuits.

	Total	Periods 45
Suggestive Assessment Methods		
<b>Continuous Assessment Test</b>	Formative Assessment Test	End Semester Exams
(30 Marks)	(10 Marks)	(60 Marks)
1. Description Questions	1. Assignment	1. Description
<b>2.</b> Formative Multiple Choice	2. Online Quizzes	Questions
Questions	3. Problem Solving	<b>2.</b> Formative Multiple
	Activities	Choice Questions
Outcomes		

Upon completion of the course, the students will be able to:

- Design MOS single stage, multistage amplifiers. CO602.1
- CO602.2 Analyze Stability in MOS amplifiers.
- CO602.3 Carry out transistor level design of the most important building blocks used in digital CMOS VLSI circuits.
- Discuss design methodology of arithmetic building block. CO602.4

CO602. 5 Analyze tradeoffs of the various circuit choices for each of the building block.

#### **Text Books**

- 1. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", McGraw Hill, 2000
- 2. Jan Rabaey, Anantha Chandrakasan, B Nikolic, "Digital Integrated Circuits: A Design Perspective". Second Edition, Feb 2003, Prentice Hall of India

#### **Reference Books**

1. N.Weste, K. Eshraghian, "Principles of CMOS VLSI Design". Second Edition, 1993 Addision Wesley.

2.Philip E.Allen, "CMOS Analog Circuit Design", Oxford University Press, 2013

3.Paul R.Gray, "Analysis and Design of Analog Integrated Circuits", Wiley Student edition, 5th edition, 2009.

4.R.Jacob Baker, "CMOS: Circuit Design, Layout, and Simulation", Wiley Student Edition, 2009

#### Web Resources

- 1. https://nptel.ac.in/
- 2. https://nptel.ac.in/courses/117/106/117106030/
- 3. https://onlinecourses.nptel.ac.in/noc20\_ee05/preview

#### CO Vs PO Mapping and CO Vs PSO Mapping

CO	PO1	PO2	PO3	PO4	PO5	PO6	<b>PO7</b>	PO8	<b>PO9</b>	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	3			2											
2	3	2											3		
3	3	2													
4	3												2		
5	3	2												1	
6	1			2								3			

#### $1 \rightarrow Low 2 \rightarrow Medium 3 \rightarrow High$

21VL1603	
	ADVANCED DIGITAL SYSTEM DESIGN

L T P C 3 0 0 3

#### Prerequisites for the course

• Digital Electronics.

#### Objectives

- To get an idea about designing complex, high speed digital systems and how to implement such design.
- To understand the mapping algorithms into architectures
- To analyse the combinational network delay

<ul><li>To design</li><li>To study t</li></ul>	the sequencing stat	ay subsystems				
UNIT I	MAPPING AL	GORITHMS INTO ARCHITECT	URES	9		
Data path synthes	is, control structure	s, critical path and worst case timing	analysis.	FSM and Hazards.		
UNIT II	COMBIN	NATIONAL NETWORK DELAY		9		
Power and energy for clocking. Perf	y optimization in co ormance analysis.	ombinational logic circuit. Sequentia	al machin	e design styles. Rule		
UNIT III	SEQU	JENCING STATIC CIRCUITS		9		
Circuit design of circuits. Synchron	latches and flip-flonizers.	ops. Static sequencing element meth	nodology.	Sequencing dynami		
UNIT IV	DATA PA	ATH AND ARRAY SUBSYSTEMS	S	9		
Addition / Subtr ROM, serial acce	action, Comparator ss memory, context	s, counters, coding, multiplication addressable memory	and divis	ion. SRAM, DRAM		
UNIT V	RECO	ONFIGURABLE COMPUTING		9		
partially reconfig	urable, Pipeline reco	onfigurable, Block Configurable, Par	allel proc	essing.		
C		Total I	Periods	45		
Continuous Ass (30 Mark	essment Methods essment Test s)	Formative Assessment Test (10 Marks)	End Semester Exams (60 Marks)			
<ol> <li>Description</li> <li>Formativ</li> <li>Questions</li> </ol>	on Questions e Multiple Choice s	<ol> <li>Assignment</li> <li>Online Quizzes</li> <li>Problem Solving Activities</li> </ol>	1. ] 2. ]	Description Questions Formative Multiple Choice Questions		
Outcomes						
Upon completio	on of the course, t	he students will be able to:				
CO603.1 I	dentify mapping alg	gorithms into architectures.				
CO603. 2	Summarize various o	lelays in combinational circuit and it	s optimiz	ation methods		
CO603. 3	Summarize circuit d	esign of latches and flip-flops.				
CO603.4 (	Construct combinati	onal and sequential circuits of mediu	ım compl	exity that is based		
	on VLSIs, and progr	ammable logic devices.				
CO603. 5 S	econfigurable, Pipe	line reconfigurable architectures and	block co	, partially nfigurable.		
Text Books						
1. W.Wolf, '	FPGA- based Syste	m Design", Pearson, 2004.				
<ol> <li>N.H.E.We</li> <li>S.Hauck&amp;</li> <li>computati</li> </ol>	este, D. Harris, "CM A.DeHon, "Recon on", Elsevier, 2008.	OS VLSI Design (4th edition)", Pear figurable computing: the theory	rson, 2010 and prac	0. tice of FPGA-base		
1						

- 1. F.P. Prosser & D. E. Winkel, "Art of Digital Design", 1987.
- 2. R.F.Tinde, "Engineering Digital Design", (2nd edition), Academic Press, 2000.
- 3. C. Bobda, "Introduction to reconfigurable computing", Springer, 2007.
- 4. M.Gokhale & P.S.Graham, "Reconfigurable computing: accelerating computation with field-programmable gate arrays", Springer, 2005.
- 5. C.Roth," Fundamentals of Digital Logic Design", Jaico Publishers, 5th edition., 2009.

#### Web Resources

- 1. https://www.coursera.org/learn/digital-systems
- 2. <u>https://nptel.ac.in/courses/108/106/108106177/</u>
- 3. <u>https://youtu.be/M0mx8S05v60</u>
- 4. <u>https://youtu.be/vsoYlH1 hbc</u>
- 5. https://www.udemy.com/course/learn-digital-system-design-module-1-from-basics/

#### CO Vs PO Mapping and CO Vs PSO Mapping

CO	PO1	PO2	PO3	PO4	PO5	PO6	<b>PO7</b>	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	3	3	3	3	3						2	2		1	
2	3	3	3	3	3						2	2	2		
3	3	3	3	3	3						2	2			
4	3	3	3	3	3						2	2	2		
5	3	3	3	3	2						2	2	1		

#### $1 \rightarrow Low 2 \rightarrow Medium 3 \rightarrow High$

21CS1605	RESEARCH METHODOLOGY FOR ENGINEERS	L	Т	Р	С
		3	0	0	3

#### Prerequisites for the course

## NIL

#### Objectives

- 1. To understand some basic concepts of engineering research and its methodologies.
- 2. To identify various sources of information for literature review.
- 3. To familiarize the various procedures for analysis and optimization of research techniques
- 4. To understand report writing and presentation skills.
- 5. To understand about intellectual property rights

UNIT I	INTRODUCTION TO RESEARCH METHODOLOGY	9
Research –types	of research-research process, engineering research- ob	ojectives, motivation,
types,research ques	tion, formulating a research problem	
UNIT II	LITERATURE REVIEW	9

N 1E:	TZ 1 1 A 1		(' D'I	1' 1' D ( 1
New and Existing	Knowledge, Analy	sis and Synthesis, Types of Publica	tions, Bit	bliographic Databases,
Measures of Resea	rch impact, keywo	ords, Types of Plagiarism, Software	Used for	Identifying Plagiarism
Techniques to Avo	id Plagiarism, eth	ics in engineering research		r
UNIT III	ANA	LYSIS AND OPTIMIZATION		9
Research tools, Sta	atistics-one dimens	ional, two dimensional, multidimens	sional, Op	ptimization Methods –
Two parameter, mu	ulti parameter, cost	function. Survey research methods		
UNIT IV	TECHNI	CALWRITING /PRESENTATION	N	9
Technical writing	– attributes and re	easons, writing strategies, Journal F	aper: Str	ructure and Approach,
Language Skills, W	Vriting Style, and E	Editing, Rules of Mathematical Writing	ng <b>,</b> Attrik	outions and Citations,
Acknowledgment	s, patents.			
UNIT V	INTELI	LECTUAL PROPERTY RIGHTS		9
Introduction, Signi	ficance, Requirem	ents for Patentability, Application P	reparation	n and Filing, Forms of
IPR, IPR and Licer	nsing, patent – exa	mples		-
		Total I	Periods	45
Suggestive Asses	sment Methods			
Continuous Asse	ssment Test	Formative Assessment Test	End Se	mester Exams
(30 Marks)		(10 Marks)	(60 Ma	rksj
1.Description Que	estions	1.Assignment	1.Descr	iption Questions
2.Formative Multi	iple choice	2.Online Quizzes	2.Form	ative Multiple choice
questions		3.Problem solving Activities	questio	ns
Outcomes				
Upon completion	n of the course, t	he students will be able to:		
CO911.1 De	emonstrate the con	cepts of engineering research and its	methodo	logies.
CO911. 2 Ui	nderstand the vario	ous methods used to collect the data f	or researc	ch.
CO911.3 Fo	ormulate appropria	te research problem and conduct the	experime	ents using analysis
an	d optimization			
CO911.4 W	rite quality researc	h in engineering.		
CO911. 5 Ui	nderstand the conc	epts of intellectual property rights.		
Text Books				
1. Dipar	nkar Deb, Rajeeb I	Dey, Valentina E. Balas."Engineering	Research	h Methodology A
Practi	ical Insight for Res	earchers", Springer. 2019	•	: : : : : : : : : : : : : : : : : : :
2. David	l V. Iniel, "Resear	n Methods for Engineers", cambridg	$x \wedge Proof$	sity press, 2014
3. Villaya	ak Ballagi Mousal	2019	y A Flaci	ical Allu Scientific
, ippro	such , ence mess,	2017		
<b>Reference Books</b>	5			
1. RanjitKuma Fifth edition	ar, "Research Meth n,2019	odology a step-by-step guide for beg	ginners" S	SAGE publications,
Web Resources				
• <u>http</u>	ps://nptel.ac.in/	<u>courses/107/108/107108011/</u>		
• <u>htt</u>	os://onlinecours	ses.swayam2.ac.in/cec20_hs17/j	<u>preview</u>	
CO Vs PO Mapping a	and CO Vs PSO Ma	pping		

Franc	ris Xavi	er Eng	ineerin	g Colle	ge   De	partmei	nt of E <b>C</b>	CE /M.1	E-VLSI	R2019	/ Curric	ulum	and Sy	yllal	bi 2021	20
CO	PO1	PO2	PO3	PO4	PO5	PO6	<b>PO7</b>	PO8	PO9	PO10	PO11	PO12	2 PS	01	PSO2	PSO3
1	3	3	1								3	3	2	2	1	1
2	3	3	1								3	3	2	2	1	1
3	3	3	1								3	3	2		1	1
4	3	3	1								3	3	2	2	1	1
5	3	3	1								3	3	2	2	1	1
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21V	L161	1		Adva	nced I	Digital	Syster	m Desi	ign La	borator	у	_	L	T	P	C
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Dig	ital El	ectron	ics, VI	SI Des	sign											
Obj	ective	S			0											
	1. То рт	unders	stand c	omple	x comb	oination	nal circ	cuits us	sing HI	DL at be	haviora	l, stru	ctural	and		
	2. To	unders	stand c	omple	x seque	ential c	rcuits	using	HDL a	t behav	ioral, sti	ructura	l and	RTI	L levels	
-	3. To	write t	the test	bench	les to s	imulate	e comb	vination	nal and	sequen	tial circ	uits.				
2	4. To	Learn	how the	ne lang	uage ii	$\frac{1}{2} \int \frac{1}{2} \int \frac{1}$	ardwar	e and l	helps to	o simula	ite and s	ynthe	size th	e di	gital sy	stem
S.N	5. 10 0		st of E	xperin	using r ients	TUAS	withi	especi	to spec	eu anu a	llea.		CO			
				L												
Usir	ng Veri	ilog co	de des	ign, sii	nulate	and sy	nthesiz	ze the f	followi	ng with	a suitał	ole FP	GA.			
-	1.	8 to	o 3 pro	gramn	nable p	riority	encod	ers.					CO1			
,	2.	Fu	ll Adde	er using	g struct	ural m	odelin	g					CO1			
Í	3.	Fli	p Flop	s (D, S	R, T, J	K)							CO2	1		
4	4.	3-t	oit arbi	trary C	ounter	, 4 bit l	binary	up/dov	wn/up-	down co	ounter w	vith	CO2	1		
	5.	Sec	quentia	l block	to det	$\frac{1}{2}$ ect a s	equenc	ce (say	11101	) using	appropr	iate	CO2			
	6.	FS	M 8-b	it ripp	le carry	<sup>7</sup> adder	and ca	arry sk	ip adde	er			CO3	•		
,	7.	8-t	oit Carı	y Sele	ct Add	er							CO3			
1	8.	8-t	oit Seri	al, Par	allel M	ultiplie	er and	genera	te repo	ort on ar	ea and		CO3			
9	9.	De	velop	the bel	naviou	al styl	e HDI	code	for 4-	bit cour	ter.Dev	elop	<b>CO4</b>			
		the	struct	ural sty	le HD	Lcode	for 4-ł	oit cou	nter us	ing T Fl	ip Flop	(use				
		of Co	genera mpile.	te stat synthe	tement, esize a	, area- nd sim	performulate e	mancea each de	analysi esign e	s atter ntity an	synthes d verify	1ze).				
		fur	ictiona	lity by	creatir	igvecto	or wav	eform	file.	2	5					
Usir	ng Syst	em Ve	erilog c	ode, s	imulate	the fo	llowin	g								
	10.	Ful	ll Subt	ractor	using s	tructur	al mod	leling					CO4			
	11.	Fli	p Flop	s (D, S	R, T, J	K)							CO5			

Francis	Xavi	er Engi	ineering	g Colleg	ge   Dej	partmen	nt of EC	CE /M.I	E-VLSI	R2019	/ Curric	ulum ar	nd Sylla	bi 2021	21
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Sugg	estive	Asses	sment	Meth	ods										
Lab	Comp	onent	s Asse	ssmen	ts					End Se	mester	Exams			
(50 N	Aark	s)							(	(50 Mar	rks)				
1 Exr	erim	ent													
2.Mo	del la	b exan	1						-	1.End se	emester	lab exar	n		
Outc	omes														
Upor	n con	pletio	n of th	ne cou	rse, the	e stude	ents wi	ill be a	ble to:	}					
Labo	rator	y Req	uirem	ents											
CO61 RTL	1.1. l levels	Design	and m	nodel c	omplex	k comb	vinatio	nal circ	cuits us	ing HD	L at beł	navioral,	structu	ral and	
CO61 levels	1.2. ]	Design	and m	nodel c	omplex	k seque	ential c	ircuits	using	HDL at	behavio	oral, stru	ictural a	nd RTL	
CO61	1.3. ]	Develo	p the t	est ben	ches to	o simul	late co	mbinat	ional a	and sequ	ential c	ircuits.			
CO61	1.4. ]	Learn l	now the	e langu	age in	fers ha	rdware	e and h	elps to	simulat	te and s	ynthesiz	e the di	gital	
syster	n.	mnlan	aant an	d anal	uzo the	digita	1 eveta	me nei	ng FD(	A a wit	h racnac	ot to sno	ad and a	rag	
0001	1.5.1	mpien		iu anai	yze the	uigita	I Syste	ins usi		JAS WIL	ii iespec	t to spec		iica.	
Refer	ence	Books	6												
1. P	eter J	. Ashe	nden, '	"Digita	l Desi	gn: An	Embe	dded S	Systems	s Appro	ach usir	ng Verilo	og", Els	evier, 20	010.
2. Sai	nir Pa	alnitka	r, "Vei	ilog H	DL: A	Guide	to Dig	gital Do	esign a	nd Synt	hesis", l	Pearson	Educati	ion, 2nd	
Editio	on, 20	10.					7t	. <b>V</b>	f (	C:		Countly a m	:		
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Platfo	orm. F	First Ec	lition.	2017.		IIOA	Desig		are sp		penden	it i uons	ning		
Web	Resc	ources	; ;												
1.	htt		nptel.a	c.in/c	ourses	/117/	105/1	17105	5080/						
2.	htt	ps://v	ww.x	ilinx.co	om/su	, pport,	, /docur	nenta	, tion/s	w_manu	uals/xil	inx2020	)_2/ug8	388-viva	ado-
	des	ign-flo	ows-ov	verviev	w-tuto	rial.pc	lf								
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	Des	sign/2	015x/	VHDL	/docs-	pdf/V	ivado_	Tutor	ial.pdf						
CO Vs	: PO N	Ларрії	ng and	CO Vs	: PSO N	<i>l</i> appir	ıg								
			2				2								
CC	PO	PO	PO	PO	PO	PO	PO	PO	PO	<b>PO1</b>	PO1	<b>PO1</b>	PSO	PSO	PSO
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co	РО	PO	РО	РО	PO	PO	РО	РО	РО	PO1	PO1	<b>PO1</b>	PSO	PSO	PSO
CO	1	2	3	4	5	6	7	8	9	0	1	2	1	2	3
1	1		2							2					
2	2									2			3		
3		2												1	
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#### SEMESTER II

S.No.	Course Code	Course	Category	Contact Periods		Т	Р	С
Theory	y Courses	-					_	-
1	21VL2601	Low Power VLSI Design	PC	3	3	0	0	3
2		Professional Elective III	PE	3	3	0	0	3
3		Professional Elective IV	PE	3	3	0	0	3
4		Professional Elective V	PE	3	3	0	0	3
5		Professional Elective VI	PE	3	3	0	0	3
Theory	y cum Pract	ical Courses						
1	21VL2602	IC Design for Communications	PC	5	3	0	2	4
Practic	cal Courses				•	•		
1	21VL2611	Analog and Digital IC Design Laboratory	PC	4	0	0	4	2
2	21VL2911	Advanced Design and Analysis Laboratory	EEC	4	0	0	4	2
			Total	28	18	0	10	23
21V	L2601	LOW POWER VLSI DE	SIGN		L	T	P	C
Droroc	uicitos for	the course		•	3	0	0	3
•	CMOS VLS	I Design						
Object	ives							
1.	Identify sour	rces of power in an IC.						
2.	To identify t	he power dissipation mechanisms in vario	ous MOS logi	c styles				
3.	To familiariz	ze suitable techniques to reduce power dis	sipation	-				
4.	To know the	e design concepts of micro sensors and mi	cro actuators.					
5.	To familiariz	ze concepts of quantum mechanics and na	no systems.					
U	NIT I	POWER DISSIPATION IN	CMOS			ç	)	
Physics	of power d	issipation in CMOS FET devices - Sou	rces of powe	r consum	ption	– Sta	atic P	ower
Dissipa	tion, Active	Power Dissipation - Basic principle of lo	w power des	ign, Need	for lo	w po	ower `	VLSI
chips, S	Sources of po	ower dissipation on Digital Integrated circ	uits, Emergin	g Low po	wer ap	proa	aches.	
UN		POWER OPTIMIZAT	ION			ç	)	
	·							

Logic level power optimization – Cit	cuit level low power design – Standa	ard Adder Cells	s, CMOS Adders
Architectures-BiCMOS adders - Lov	w Voltage Low Power Design Tech	niques, Current	t Mode Adders -
Types Of Multiplier Architectures,	Braun, Booth and Wallace Tree Mu	ltipliers and the	heir performance
comparison			
UNIT III DESIGN O	FLOW POWER CMOS CIRCUIT	ГS	9
Computer arithmetic techniques for	low power system low voltage lo	w power static	Random access
and dynamic Random access memor	ies _ low power clock Inter connect	and layout de	sign = Advanced
techniques	ies – low power clock, inter connect	and layout de	sign – Auvanceu
teeninques			
UNIT IV	POWER ESTIMATION		9
Power Estimation techniques – logic	power estimation – Simulation power	er analysis –Pro	obabilistic power
analysis.			
	SPECIAL TECHNIOUES		9
Power Reduction in Clock networks	CMOS Floating Node, Low Power	Bus Delay bal	ancing, and Low
Power Techniques for SRAM.	,		
	Total I	Periods	45
Suggestive Assessment Methods			
<b>Continuous Assessment Test</b>	Formative Assessment Test	End Semest	er Exams
(30 Marks)	(10 Marks)	(60 Marks)	
1. Description Questions	1. Assignment	I. Descr	iption
2. Formative Multiple Choice	2. Unline Quizzes	Quest	1005 ativo Multiplo
Questions	Activities	2. FOIIII Choic	e Questions
Outcomes	neuvities	Choice	e questions
Upon completion of the course, t	he students will be able to:		
CO601.1 Identify the sources	of power dissipation in digital IC sys	tems	
CO601.2 Understand the impa	act of power on system performance	and reliability	
CO601.3 Understand leakage	sources and reduction techniques	5	
CO601. 4 Recognise advanced	l issues in VLSI systems, specific to	the deep-subm	nicron silicon
technologies		I I I I I I I I I I I I I I I I I I I	
CO601. 5 Identify the mechan	isms of power dissipation in CMOS i	ntegrated circu	iits
Text Books			
1. Abdelatif Belaouar, Mohamed	I.Elmasry, "Low power digital VLSI	design", Kluw	ver, 1995.
2. A.P.Chandrasekaran and R.W.	Broadersen, "Low power digital CM	OS design", Kl	uwer,1995.
Reference Books			
1. Dimitrios Soudris, C.Pignet, C	Costas Goutis, "Designing CMOS Cir	cuits for Low	Power" Kluwer,
2002.			
2. Gary Yeap, "Practical low pow	ver digital VLSI design", Kluwer, 199	98.	
3. Kaushik Roy and S.C.Prasad, 4	'Low power CMOS VLSI circuit des	ign", Wiley, 20	000.
4. Tai Ran Hsu ,"MEMS and Mic	crosystems Design and Manufacture"	,Tata Mcraw I	Hill, 2002.

5. Anatha P Chandrakasan, Robert W Brodersen, Low power digital CMOS Design, Kluwer Academic, 1995

6. Christian Piguet, Low power CMOS circuits, Taylor & Francis, 2006

#### Web Resources

- 1. <u>https://www.youtube.com/watch?v=TF001JAll2Y</u>
- 2. <u>https://www.intechopen.com/books/very-large-scale-integration/low-power-design-methodology</u>
- 3. https://nptel.ac.in/courses/106/105/106105034/

CO Vs PO Mapping and CO Vs PSO Mapping

	-	-		-	-			-		-					
C <b>O</b>	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	3		3	3	2	3		3	2				2		
2					3	3			1					1	
3			2	3	2			2	1		2				
4				3	3	2			1				1		
5			3	3	3	2			2						
	1→Lo	$w 2 \rightarrow$	Mediu	ım 3→	High										
	4111.0							COM			NG		-		
2	1VL2	602			IC D	ESIGN	FOR	COM	MUNI	CATIO	NS			$\begin{array}{c c} T & P \\ \hline 0 & 0 \end{array}$	C
													3	0 2	4
P	rereq	uisite	s for t	he cou	ırse										
		Analog	g and D	Digital	IC Des	ign									
C	<b>)bject</b> i	ives													
	1. '	To und	erstand	d the b	asics of	f wirele	ess con	nmunica	ation						
	2. 7	To Gai	n the b	asic K	nowled	lge of I	Low no	oise Am	plifier.						
	3. '	To Stu	dy the	Transr	nitter a	rchitect	ture an	d Powe	er ampli	fier.					
	4. ′	To ana	lyze th	e Rece	iver ar	chitectu	are for	wireles	s Com	nunicat	ion				
	5. 7	To und	lerstan	d the v	arious	types o	f mixe	rs desig	gned for	wireles	ss comn	nunicatio	on, and	to intro	duce
	1	the app	olicatio	ns of f	requen	cy synt	hesizei	ſS.							
U	UNIT I				C	OMMU	JNICA	TION	CONC	CEPTS			9		
C	Vervie	w of V	Wireles	ss Syst	ems, A	Access ]	Metho	ds, Mo	dulatior	n Schem	nes, Wi	reless C	hannel	Descrip	tion,
P	ath Lo	ss, Mu	ltipath	Fading	g: Chai	nnel Mo	odel an	d Enve	lope Fa	ding, Fi	requenc	y Select	ive and	Fast Fa	ding
U	INIT II	[	TF	RANSN	IITTE	R ARC	HITEC	TURE	AND P	OWER	AMPLI	FIER	9		
Т	ransm	itter B	ack E	nd, Qu	ıaderat	ure LC	) gene	rator-S	ingle e	nded R	C and	LC, R-	C with	Differe	ntial
S	tages;	power	ampl	ifier d	esign-	specif	ication	s, pow	er outp	put con	trol, PA	A desig	n issue	s, Class	s A,
A	B/B/C	C/E amp	plifiers												
_								<b>D</b> (1							
U	INIT II	I			R	ECEL	VER A	RCHI	TECT	URES			9		

Receiver Front End: General Design Philosophy, Super heterodyne and Other Architectures, Filter Design: Band Selection Filter, Image Rejection Filter, Channel Filter; Design parameters: Nonlinearity, Harmonic Distortion, Intermodulation, Gain compression, Blocking; Derivation of NF and IIP3 of Receiver Front End, Partitioning of receiver NF and IIP3 into individual stages

**UNIT IV** 

LOW NOISE AMPLIFIER

9

Introduction, CS, CG, Cascaded and cascoded configurations of LNA, Wideband LNA Design, Narrow Band LNA: Impedance Matching, Core Amplifier

UNIT V MIXER AND FREQUENCY SYNTHESIZER

9

Mixer: Passive Down Conversion Mixers, Active Down conversion Mixers, Up conversion Mixers; Frequency synthesizer: PLL-based frequency synthesizer- phase detector- dividers- Oscillators- Loop filter- first-order, second order- higher order filters

S.No		List of Experiments	CO
1.	Introduction to Ca analysis and power	dence tool, schematic editor, ADE tool, r analysis.	, transient CO1
2.	Schematic design amplifiers	and transient analysis of CS and CG sir	ngle stage CO1
3.	Construction of tw analysis, NF and C	o stage CS cascaded LNA with transient	t CO2
4.	Design of cascaded analysis	LNA with NF, Gain, Linearity (IIP3 ar	nd P1dB) CO2
5.	Maximum-Power-	Gain Output Impedance Matching	CO3
6.	Stability Analysis	and Source/Gate Degeneration	CO3
7.	Maximum-Power-	Gain Input Impedance Matching	CO4
8.	Minimum-Noise-F	igure Input Impedance Matching	CO4
9.	Design and simula	tion of Class A, B Power Amplifiers	CO4
10.	Class AB, C, E por	wer amplifiers	CO5
11.	Design and analysi	is of active/passive down conversion mix	xer CO5
12.	Construction and a	nalysis of up conversion mixer	CO5
Total Perio	ds		45 Theory +15 Lab
Laboratory	Requirements		·
Cadence Vir	rtuoso, RF Spectre		
Suggestive	Assessment Method	S	
Continuous	Assessment Test	Lab Components Assessments (20 Marks)	End Semester Exams

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T	ext Bo	oks													
	1. E	losco I	Leung,	"VLS	I for W	Vireles	s Com	munica	tion",	2nd edi	tion, Sp	ringer p	oublicat	ions, Ca	nada,
	2	011.													
	2. E	8.Raza	vi, "RF	' Micro	oelectro	onics",	Pearso	on Edu	cation,	2013.					
R	eferer	ce Bo	oks												
	3. E	)avid '	Tse ar	id Pra	modVi	swana	th, "F	undam	entals	of Wir	eless C	ommun	ication"	', Camb	ridge
	P	ress, 2	005.												
	4. E	.Raza	vi, "Fu	ndame	ntals o	f Micr	oelectr	onics"	, Wiley	, 2013.					
	5. F	ábio P	, Elise	nda R,	, Rafae	el C.L	, Fran	cisco V	/.F, "A	utomate	ed Hier	archical	Synthe	sis of R	adio-
	F	requer	ncy Inte	egrated	l Circu	its and	System	ms", Sp	oringer	, 2020					
W	'eb Re	sourc	es												
	1. F	FIC D	esign,	http://v	www.e	e.scu.e	edu/cla	sses/20	004win	ter/elen	351/lect	ure1.pd	f		
	2. A	dvanc	ed RF	and A	Analog	Integr	ated C	ircuits	for Fo	ourth Ge	eneratio	n Wirel	ess Cor	nmunica	utions
	a	nd Bey	ond, h	ttps://c	downlo	ads.hi	ndawi.	com/jo	urnals/	speciali	ssues/42	27619.p	df		
	3. V	Vireles	s Con	ımunic	ation 1	ICs, ht	tps://w	ww.ak	.con	n/in/en/p	oroducts	s/commu	inicatio	n-ic/wire	eless-
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CO	PO1	PO2	PO3	PO4	PO5	PO6	<b>PO7</b>	PO8	<b>PO9</b>	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	3													2	
2	1	2		2											
3	2												1		
4	3	2	3										2		

1→Low 2→Medium 3→High

	2611	ANALOG AND DIGITAL IC DESIGN LABORATORY	L	Т	Р	C
			0	0	4	2
Prere	equisites	for the course				
Digit	al System	Design Laboratory				
Objeo	ctives					
The st	udent shou	ıld be made:				
1. 2. 3. 4. 5.	To learn To learn To famil To provi To get th	Hardware Descriptive Language (Verilog/VHDL) the fundamental principles of VLSI circuit design in digital and iarize fusing of logical modules on FPGAs de hands on design experience with professional design (EDA) p he basic idea about analog and digital system design	analo olatfoi	g dor rms	nain	
S.No	List of E	xperiments	CO	1		
EXPE	RIMENTS	S PART I: Digital System Design using HDL and FPGA				
1.	Design a Xilinx/A	Universal Shift Register using HDL. Simulate it using Itera Software and implement by Xilinx/Altera FPGA	CC	)1		
2.	Design F using Xil	inite State Machine (Moore/Mealy) using HDL. Simulate it inx/Altera Software and implement by Xilinx/Altera FPGA	CC	)2		
EXPE	RIMENTS	S PART II: Digital Circuit Design				
3.	Design a	nd simulate a CMOS inverter using digital flow	CC	)3		
4.	Design a	nd simulate a CMOS Basic Gates and Flip-Flops	CC	)3		
5.	Design a	nd simulate a 4-bit synchronous counter using a Flip-Flops	CC	)4		
	Manual/	Automatic Layout Generation and Post Layout Extraction for par	rt II e	xperi	ments	•
	Analyze Layout S	the power, area and timing for part II experiments by performing imulations.	g Pre	Layo	ut and	l Post
EXPE	RIMENT	S PART III: Analog Circuit Design				
6.	Design a	nd Simulate a CMOS Inverting Amplifier.		15		
7.	Design a Common	nd Simulate basic Common Source, Common Gate and Drain Amplifiers.	CC	)5		
Analy	ze the inpu	at impedance, output impedance, gain and bandwidth for the abo	ve tw	o exp	perime	ents b
perfor	ming Sche					

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2.N	Model	lab exa	am						1.		licster id	io chain			
Ou	itcom	es													
At	the en	d of th	e cour	se, the	studen	t shoul	ld be a	ble to:							
	CO6 CO6 CO6 CO6	11.1. V 11.2. I 11.3. S 11.4. I 11.5. S	Vrite F mport Synthes Design Simulat	IDL co the log size Pla the lay te the la	de for ic mod ace and outs of avouts	basic a lules in l Route f Digita of Dig	as well nto FPC the di al and ital and	as adv GA Boa gital II Analog d Analog	anced ards Ps g IC Bl og IC J	digital i ocks us Blocks 1	ntegrate ing ED 1sing EI	ed circui A tools DA tools	t		
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	2. X	Cilinx/A	Altera/	equival	lent FP	GA Bo	pards 1	0 no	• •		Toola 1	0 Usor 1	liconso		
<b>Re</b>	3. C 4. P feren	ersona ce Bo	l Com oks ste . D	psis/ N puter 2 avid N	lentor 0 no	Harris	-CMO	s VLSI	Desig	nt EDA	cuits an	d Svste	ms Pers	spective	2
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Re           1.N           For           2.1           We           0           0           0           1           2           3	3. C 4. P feren Neil H. urth E Design eb Re 1. h ci 2. h a. 3. h rs PO N PO 1 3 2 2 2	adence ersona ce Bo E. We Edition n Verif sourc ttps:/, nalog- ttps:/, Mappin PO 2 3 2 3	oks l Com oks ste , D ,2011 ication es /resou -in-yo /www rf-flov /web.i ng and 3 PO 3 2	avid M avid M n with urces.p ur-layo c.caden vs.htm tu.edu l CO Vs PO 4	Ioney I Ioney I E. by S cb.cad out ce.con I .tr/~a s PSO N <b>PO</b> 5	Harris Samir I ence.c n/ko_F teserd Aappir 6	-CMO Palnitk om/bl (R/hou (/CAD)	S VLSI car, Pro og/20 me/too ENCE%	Desig entice 19-wc ols/cu 620Ma <b>PO</b> 9	n-A Ciro Hall , 2 orking-v stom-ic anual.po PO1 0	cuits an 003 with-an c-analog df 1	alog-vs g-rf-des	ms Pers -digital- ign/cus PSO 1 2	-integra stom-ic-	e, ited- 3 1
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## $1 \rightarrow Low 2 \rightarrow Medium 3 \rightarrow High$

21VL29	011	Advanced Design and Analys	is Laboratory	L	Τ	Р	C
				0	0	4	2
Prerequ	isites for t	the course					
Digital	System De	sign Laboratory					
Objecti	ves						
1. To Co	onceptualiz	e a novel idea / technique					
2. To U	se EDA too	ol to design complex combinational and	sequential circuits.				
3. To U	nderstand t	he management techniques for implement	ntation of the circuits				
4. To D	esign the co	omplex combinational and sequential log	ic circuits using various	cons	struct	s in	
Cadence	e and kit.						
5. To In	nplement th	ne design using Xilinx and ALTERA FP	GAs.				
S.No	List of E	xperiments		CC	)		
51110				00			
1.	Design M Cyclone	IIPS 32-Bit RISC Processor and implem V FPGA and Study about it's performa	ent it using ALTERA	C	01		
2.	Design a	Reconfigurable FIR Filter and verify it's	functionality through Cyclone IV FPGA	C	01		
3.	Design ar	ad Implementation of Smart Traffic Light road using ALTERA Cyclone IV FPGA	t System for congested	C	02		
4.	Design ar Cyclone 1	nd Implementation of CORDIC Algorith	m using ALTERA	C	02		
5.	Design a character	MOS based SRAM cell using 180 nm te	chnology and verify its	C	03		
6.	Design N character	OR gate using Domino logic CMOS invistics.	erter and verify its	C	03		
7.	Design C its charac	MOS transmission gate and perform all teristics.	he analysis to verify	C	D4		
8.	Design X verify its	OR and XNOR gate using dynamic CM characteristics.	OS logic circuits and	C	04		
9.	Design La Monte Ca	ayout of CMOS inverter and perform po arlo analysis, Corner analysis and etc.	st layout analysis,	C	05		
10.	Design ar technolog	by one of the combinational logic circuit by and verify the circuit using transient a	using 180 nm nalysis	C	05		
11.	Design and verify	y one of the sequential logic circuit using transient analysis	g 180 nm technology	C	05		
Total P	eriods :60			<u>I</u>			
Suggest	ive Assess	ment Methods					
Lab Co (50 Ma	mponents rks)	Assessments	End Semester Exam (50 Marks)	S			
1.Exper	iment		1.End semester lab example.	am			
2.1010UC							

#### Outcomes

#### Upon completion of the course, the students will be able to:

CO911.1. Conceptualize a novel idea / technique

CO911.2. Use EDA tool to design complex combinational and sequential circuits.

CO911.3. Understand the management techniques for implementation of the circuits

CO911.4. Design the complex combinational and sequential logic circuits using various constructs in Cadence and kit.

CO911.5. Implement the design using Xilinx and ALTERA FPGAs.

#### **Laboratory Requirements**

ALTERA Cyclone IV FPGA-10 Nos Cadence -10 Users Xilinx

#### **Reference Books**

1.Neil H. E. Weste, David Money Harris -CMOS VLSI Design-A Circuits and Systems Perspective, Fourth Edition,2011

2. Digital Integrated Circuits a Design Perspective-Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic

#### Web Resources

- 1. https://web.itu.edu.tr/~ateserd/CADENCE%20Manual.pdf
- 2. https://www.xilinx.com/support/documentation/sw\_manuals/xilinx2020\_2/ug888-vivado-design-flows-overview-tutorial.pdf
- 3. https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/manual/intro\_to\_qua rtus2.pdf

CO Vs PO Mapping and CO Vs PSO Mapping

CO	PO	PO	PO	PO	PO	РО	РО	PO	PO	РО	РО	PO1	PSO	PSO	PSO
CO	1	2	3	4	5	6	7	8	9	10	11	2	1	2	3
1	3														
2	2		3										2		
3	2	2	2										3		
4	3													1	
5	1		3												

1→Low 2→Medium 3→High

#### SEMESTER III

S.No.	Cou Co	rse de	Course	Category	Contact Periods	L	Т	Р	С
Theory	cum P	ractio	cal Courses						
1	21VL	3601	Physical Design of Integrated Circuits	PC	5	3	0	2	4
2	21VL	3602	ASIC Design	PC	3	3	0	0	3
Practic	al Coui	ses							
1	21VL3	3911	Term Paper Writing	EEC	2	0	0	2	1
2	21VL	3912	Dissertation I	EEC	12	0	0	12	6
				Total	17 H + 8 W	3	0	14	14
21VL36	501		PHYSICAL DESIGN OF INTEGRAT	TED CIRCU	JITS	L	Т	P	C
						3	0	2	4
Prerequ	uisites f	or the	course			1			
• .	Analog	and D	igital IC Design						
Objecti	ves								
1. 7	To unde	erstand	the basic semiconductor device physics	of PN juncti	ons.				
2. 7	To unde	erstand	operational principles of MOSFET.						
3.	To learr	the ev	volution of MOSFET structure and Techr	nology.					
4.	Го impl	ement	the designs using front end design enviro	onment.					
5.	I'o unde	erstand	performance metrics associated with sim	nulation and	synthesis.	-			
UNITI			INTRODUCTION TO VLSI TEC.	HNOLOGY		5			
Layout	Rules-(	Circuit	abstraction Cell generation using prog	rammable lo	ogic array	transi	stor	chain	ing,
Wein-B	erger a	rrays	and gate matrices-layout of standard of	cells gate a	rrays and	sea c	of ga	tes, f	field
program	nmable	gate	array (FPGA)-layout methodologie	s-Packaging	-Computati	onal	Cor	mpley	kity-
Algorith	nmic Pa	radign	18						
UNIT I	Ι		PARTITIONING USING TOP-DOW	N APPROA	СН	5			
Partition	ning: Ap	proxi	mation of Hyper Graphs with Graphs, Ke	ernighan-Lin	Heuristic-	Ratic	-cut-	parti	tion
with cap	bacity a	nd i/o	constraints						
UNIT I	Π	FL O	ORPLANNING AND PLACEMENT	USING TO	P-DOWN	5			

APPROACH

Floor planning: Rectangular dual floor planning- hierarchical approach- simulated annealing- Floor plan sizing; Placement: Cost function- force directed method- placement by simulated annealing- partitioning placement- module placement on a resistive network – regular placement- linear placement

UNIT IVROUTING USING TOP DOWN APPROACH5Fundamentals:Maze running- line searching- Steiner trees; Global Routing: Sequential Approaches-<br/>hierarchical approaches- multi-commodity flow based techniques- Randomised Routing- One Step<br/>approach- Integer Linear Programming; Detailed Routing: Channel Routing- Switch box routing;<br/>Routing in FPGA: Array based FPGA- Row based FPGAs.

UNIT V

#### SINGLE LAYER ROUTING, CELL GENERATION AND COMPACTION

5

Lab

Planar subset problem (PSP) - Single layer global routing- Single Layer Global Routing- Single Layer detailed Routing- Wire length and bend minimization technique – Over the Cell (OTC) Routing-Multiple chip modules (MCM) - Programmable Logic Arrays- Transistor chaining- Wein-Burger Arrays-Gate matrix layout- 1D compaction- 2D compaction.

S.No	List of Experiments	СО
1.	Develop the behavioral style HDL code for 4-bit counter. Develop	CO1, CO2
	the structural style HDL code for 4-bit counter using T Flip Flop	
	(use of generate statement, area- performance analysis after	
	synthesize). Compile, synthesize and simulate each design entity	
	and verify the functionality by creating vector waveform file.	
2.	Design a traffic light controller for an intersection with a main	CO2, CO3
	street, a side street, and a pedestrian crossing (Implement it on	
	FPGA).	
3.	Design a Vending Machine (Implement it on FPGA).	CO3, CO4
4.	Using the NAND and NOR standard cells, draw the layout for D	CO4, CO5
	and SR latch. Do DRC, LVS and Extraction.	
<b>Total Periods</b>		45 Theory +15

### Laboratory Requirements

FPGA,

Xilinx,

Cadence

Suggestive Assessment Methods		
Continuous Assessment Test (30Marks)	Lab Components Assessments (20 Marks)	End Semester Exams (50 Marks)
<ol> <li>Description Questions</li> <li>Formative Multiple Choice Questions</li> </ol>	<ol> <li>Record Note</li> <li>Model Lab examination</li> </ol>	<ol> <li>Description Questions</li> <li>Formative Multiple Choice Questions</li> </ol>
Outcomes	•	

#### Upon completion of the course, the students will be able to:

- CO601. 1 Understand the basics of Semiconductor Physics
- CO601. 2 Understand working principles of MOSFET and evolution of MOSFET structure.
- CO601. 3 Use the MOSFET for DC, I-V, CV characteristics and in Analog/RF Circuit
- CO601. 4 Implement the designs using front end design environment using top down and bottom up approach.
- CO601. 5 Analyze the area, delay trade-offs and performance metrics associated with

#### **Text Books**

- 1. D.A.Neamen, Semiconductor Physics and Devices: Basic Principle, Third Edition, McGraw –Hill International, 2003.
- 2. B.G Streetman and S.K Banerjee, Solid State Electronic Devices, Seventh Edition, PrenticeHall India,2010.
- 3. Y.Taur and T.H. Ning, Fundamentals of Modern VLSI Devices, Second Edition, Cambridge University Press, 2009.

#### **Reference Books**

- 1. J. P. Collinge, FinFETs and Other Multi-Gate Transistors, Springer, 2008
- Sudeb Dasgupta, Brajesh Kumar Kaushik, Pankaj Kumar Pal Spacer, Engineered FinFET Architectures: High-Performance Digital Circuit Applications, CRC Press 2017.
- 3. S.M Sze and K.K Ng, Physics of Semiconductor Devices, Third Edition, John Wiley and Sons Inc., 2007.
- 4. Lab manuals and online manuals for tools usage and language reference manuals of HDLs.

#### Web Resources

- 1. <u>https://semiengineering.com/knowledge\_centers/eda-design/definitions/physical-design/</u>
- 2. https://www.sciencedirect.com/topics/engineering/integrated-circuit-design

#### CO Vs PO Mapping and CO Vs PSO Mapping

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	<b>PO9</b>	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	3	3													
2	3	3											2		
3	3	3													
4	3	2												1	
5	3	2													

 $1 \rightarrow Low 2 \rightarrow Medium 3 \rightarrow High$ 

				L	Т	Р	C
21VL3602		ASIC Design					
				3	0	0	3
Prerequisites for	the course						
• The pre-req	uisite knowledge	required by the students to study thi	s Course	is bas	ic kn	owled	ge in
Analog and	Digital Electronic	S S					
Objectives							
1. Explain the	types of ASIC and	typical ASIC design Flow.					
2. Give the str	idents an understa	nding of HDL coding guidelines and	synthesiz	zable F	<b>ID</b> L	constr	ucts.
3. Explain the	RTL synthesis Flo	ow with respect to different cost func	tion.				
4. Teach the v	arious timing para	meter and how to perform Static Tin	ning Anal	vsis fo	or AS	IC chi	ins.
5 Discuss the	various abstractio	n levels in physical design and guide	lines at e	ach ah	strac	tion le	vel
5. Discuss the	various abstractio	in levels in physical design and guide	innes at e	acii ao	struc		VCI.
UNIT I	ASIC D	esign Methodology & Design Flow				9	
Implementation St	rategies for Digita	LICs: Custom IC Design- Cell-base	d Design	Meth	odolo	$\int \sigma v = A$	Array
based implementation	ion approaches - T	raditional and Physical Compiler base	sed ASIC	Flow.	ouon	, 5 y 1	inay
UNIT II	Verilog	g HDL Coding Style for Synthesis				9	
HDL Coding style	- Guidelines and	Recommendation - FSM Coding C	Guideline	and C	Codin	ig Styl	e for
Synthesis							
UNIT III		RTL Synthesis				9	
RTL synthesis Flow	w – Synthesis Des	ign Environment & Constraints – Ai	chitectur	e of Lo	ogic	Synthe	esizer
- Technology Libra	ry Basics- Compo	onents of Technology Library –Syntl	nesis Opti	imizati	ion- '	Techno	ology
independent and Te	echnology depende	ent synthesis- Data path Synthesis –	Low Pow	ver Syr	nthes	is – Ti	ming
driven synthesis- F	ormal Verification	l.					
UNIT IV	Timing Pa	rameters and Static Timing Analy	sis			9	
Timing Parameter	Definition – Setup	Timing Check- Hold Timing Check	- Multicy	ycle Pa	ths-	False	Paths
- Clocking of Sync	hronous Circuits.	Fiming Analysis - Clock skew optim	– ization	Clock	Tree	Synth	iesis.
	D	Physical Design Varification				<u>,</u>	
UNII V Detailed step in D	I Avaiaal Dasian Ek	Lysical Design Vermication		d maaat		9 Condu	otina
Detailed step in Pi	iysical Design Flo	based back and design ECO. Pael	ement an	a rout	ing.	Drovo	cting
electrical overstress	Static verification	on techniques-Post-layout design veri	fication	yout is	sues	-rieve	nnng
	s. Statle vermeatio	Total	Periods		4	45	
Suggestive Asses	sment Methods		crious			10	
Continuous Asso	sment Tect	Formative Accessment Test	End So	moste	m Ev	ame	
(30 Marks)	ssment rest	(10 Marks)	(60 Ma	nieste rks)	71 LA	a1115	
1. Description	n Questions	1. Assignment	1.	Descri	ntio	n	
<b>2.</b> Formative	Multiple Choice	2. Online Ouizzes		Ouesti	ons		
Questions	F	<b>3.</b> Problem Solving	2.	Forma	tive	Multi	ple
-		Activities		<u>Choic</u> e	e Que	estion	S
Outcomes							
Upon completion	of the course, t	he students will be able to:					_

CO701.1 Analyze the different types of ASICs and design flows.

- CO701.2 Design digital systems by adhering to synthesizable HDL constructs.
- CO701.3 Synthesize the given design by considering various constraints and to optimize the same.
- CO701.4 Perform physical design by adhering to guidelines.
- CO701.5 Apprehend the importance of physical design verification.

#### **Text Books**

1. HimanshuBhatnagar, Advanced ASIC Chip Synthesis, Kluwer Academic Publisher, Second Edition, 2012

#### **Reference Books**

- 1. Erik Brunvand, Digital VLSI Chip Design with Cadence and Synopsys CAD Tools, Addison Wesley, First Edition, 2010.
- 2. J. Bhasker and RakeshChadha, Static Timing Analysis for Nanometer Designs, Springer US, First Edition, 2010.

#### Web Resources

- 1. https://www.digimat.in/nptel/courses/video/117108047/L01.html
- 2. https://nptel.ac.in/courses/118/104/118104008/
- 3. <u>https://nptel.ac.in/courses/117/108/117108047/</u>

#### CO Vs PO Mapping and CO Vs PSO Mapping

CO	PO1	PO2	PO3	PO4	PO5	PO6	<b>PO7</b>	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	3	2	1	1		1				2	1	2			
2	3	2	1	1						2	1	2	3		
3	3	2	2	1		1				2	1	2			
4	3	2	1	1						2	1	2		2	
5	3	2	2	1		1				2	1	2			

### 1→Low 2→Medium 3→High

#### **PROFESSIONAL ELECTIVES**

PROFESSIONAL	ELECTIVE I				
21VL1701	Nano-Electronic Devices and Materials	3	0	0	3
21VL1702	MEMS and NEMS	3	0	0	3
21VL1703	Flexible Electronics	3	0	0	3
21VL1704	Reliability of Devices and Circuits	3	0	0	3

Francis Xavier Engineering College   Department of ECE  M.E-VLSI   R2019   Curriculum and Syllab	2021	36
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21VL1701	NANO-ELECTRONIC DEVICES AND MATERIALS	L	Т	Р	C									
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Droroquisitos foi	r the course	3	U	U	3									
The pre-rec	usite knowledge required by the Students to study this Course	ic has	ic kn	owled	oe i									
• The pre-rec	Digital IC Design	15 Uas		lowieu	ge i									
Objectives	Digital le Design.													
6 Make stude	ants to learn the basic concents of Nano electronics													
7 Enable the	students to understand the quantum devices													
8 Enable the	students to know the tunneling devices and its uses													
9 Make the st	tudents to analyze the superconducting devices and photonics													
10 Make the st	udents to understand nano-electronic materials													
10. Wake the st	ducins to understand nano-electronic materials.													
	BASICS OF NANOELECTRONICS AND OUANTUM			9										
	DEVICES			2										
Physical fundamen	itals – basic information theory – data & bits – data processing	- Qua	ntum	n Elect	ron									
devices - Electron	s in mesocopic structures - Short channel, MOS Transistor - s	split C	Bate 7	Fransis	tor									
Electron wave tran	sistor – Electron spin transistor – Quantum Dot array – Quant	um co	mput	ter- Bi	t ar									
Qubit - Carbon Na	notube based logic gates.													
IINIT II				-										
UNITI	I UNNELING DEVICES			9										
Tunneling element	TUNNELING DEVICES z – Tunnel Effect -Tunneling Diode – Resonant Tunneling Dio	de – '	Three	9 e -Teri	mina									
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4.	Formati	ve Mu	ıltiple	Choice		5. O	nline Q	uizzes	;		Q	uestion	S	
	Question	ns				<b>6.</b> Pr	oblem	Solvir	ıg		<b>4.</b> Fo	ormativ	e Multij	ple
						A	ctivitie	S			Cl	noice Qu	uestions	S
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The pre-requ	isite knowledge	required by the Students to study thi	s Course	is bas	ic kn	owled	ge i
Physics and	electronic devices	5.					
Objectives							
1. To learn the	basics of organic	semiconductor materials.					
2. To study the	electronic device	es designed with organic materials					
3. To learn the	e concepts of fle	xible electronics and improvements	s in mate	erials	comp	atible	wit
flexible subs	trates and low-ter	mperature processing methods like p	rinting me	ethods	5		
4. To understar	nd the Thin Film	Fransistors using organic materials					
5. To study prin	nted batteries.						
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Organic devices or Sintering of metal na UNIT IV Performance on gla circuits for smart pa	n flexible substra anoparticles as co Tl ass and polymer ckaging, wearable	ate, Technologies of roll-to-roll prontacts. HIN FILM TRANSISTORS r, essential component of enabler e electronics, NFC.	inting, S	Targ	et A <sub>I</sub>	9 oplicat	tion
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Organic devices or Sintering of metal na UNIT IV Performance on gla circuits for smart pa UNIT V Batteries for low-po	n flexible substra anoparticles as co Tl ass and polymer ckaging, wearable ower flexible elect	ate, Technologies of roll-to-roll prontacts. HIN FILM TRANSISTORS r, essential component of enabler e electronics, NFC. PRINTED BATTERIES ctronics Thin, flexible, light-weight	inting, S circuitry, and in v	Targ	et Ar	9 pplica 9 9 pes, T	tion
Organic devices or Sintering of metal na UNIT IV Performance on gla circuits for smart pa UNIT V Batteries for low-po Applications: Weara	n flexible substra anoparticles as co Tl ass and polymer ckaging, wearable ower flexible electronics, s	ate, Technologies of roll-to-roll prontacts. HIN FILM TRANSISTORS , essential component of enabler e electronics, NFC. PRINTED BATTERIES ctronics Thin, flexible, light-weight mart packaging and smart card, deco	inting, S circuitry, and in v r.	Targ	et Ap	9 oplica 9 ops, T	tion tion
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CO703.1 Understnd the concepts of organic semiconductor materials.

CO703.2 Understand the organic electronic devices.

CO703.3 Learn flexible electronics and high-speed printing.

CO703.4 Learn about Thin Film Transistors.

CO703.5 Understand the concepts of paper batteries.

### Text Books

- 1. Zhenan Bao and Jason Locklin, Organic Field-Effect Transistors (Optical Science and Engineering), CRC Press, 2007
- 2. Ioannis Kymissis, Organic Field-Effect Transistors: Theory, Fabrication and Characterization (Integrated Circuits and Systems), Springer, 2009

## **Reference Books**

- 1. Qiquan Qiao (Editor), Organic Solar Cells: Materials, Devices, Interfaces, and Modeling (Devices, Circuits, and Systems), CRC Press, 2015
- 2. Christoph Brabec, Ullrich Scherf, Vladimir Dyakonov (Editors), Organic Photovoltaics: Materials, Device Physics, and Manufacturing Technologies, Wiley-VCH, 2014
- 3. Frederik C. Krebs, Stability and Degradation of Organic and Polymer Solar Cells, Wiley, 2012

## Web Resources

- 1. <u>https://www.youtube.com/watch?v=0\_FjPqBqPec</u>
- 2. <u>https://www.edx.org/course/fundamentals-nanoelectronics-part-b-purduex-nano521x</u>.
- 3. <u>https://nanohub.org/courses/fon2</u>

## CO Vs PO Mapping and CO Vs PSO Mapping

CO	PO1	PO2	PO3	PO4	PO5	PO6	<b>PO7</b>	PO8	<b>PO9</b>	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	3	3										3	1		
2	3		3									3			
3				3								3		2	
4	3				3	3						3			
5				3	3	3	3					3		1	

### $1 \rightarrow Low 2 \rightarrow Medium 3 \rightarrow High$

21VL1704	RELIABILITY OF DEVICES AND CIRCUITS	L	Т	Р	С
		3	0	0	3

### Prerequisites for the course

The pre-requisite knowledge required by the Students to study this Course is basic knowledge in Integrated circuits and electronic devices.

#### Objectives

- 1. Know the basics of Devices and their Reliability.
- 2. Understand the fundamentals of Packaging Materials, Processes and Stresses.
- 3. Know the failure and reliability of optic materials and devices.
- 4. Study the characteriastion of failure and reliability of optic materials and devices.

5. Understand	the issues and fut	ure directions of reliability.		
UNIT I	AN OVE	ERVIEW OF DEVICES & THEIR RELIABILITY		9
Electronic product	s-Historical prosp	ective, solid state devices, Integrat	ed circuit	ts, yield of electronic
products, Reliabilit survivability, Failu	ty –Brief history, l re Physics.	ong term non-operating reliability, A	Availabilit	y, maintainability and
UNIT II	PACKAGIN	NG MATERIALS, PROCESSES A STRESSES	ND	9
Introduction, IC ch	ip packaging proc	esses and .effects, solders and their l	Reactions,	Second level packin
technologies, The interconnections.	ermal stresses in	n package structures, Degradatio	n of co	ontacts and packag
UNIT III	ELECTRO O	PTICAL MATERIALS AND DEV	VICES	9
Introduction, Failu components, Relia	re and Reliability bility of optical fib	of Lasers and LEDs, Thermal de ers.	gradation	of lasers and optica
UNIT IV	FAILURE	ANALYSIS OF MATERIALS AN DEVICES	ND	9
Overview of testin	g and failure ana	llysis, Non-destructive Examination	and Dec	capsulation. Structura
characterization, ch	nemical characteriz	zation, Examining devices under elec	ctrical stre	ess.
UNIT V	FUTURE DIRI	ECTIONS AND RELIABILITY IS	SUES	9
Integrated circuit T	echnology Trends	, Scaling, Fundamental limits, Impro	oving Reli Periods	ability. <b>45</b>
Suggestive Asses	sment Methods			
Continuous Asse (30 Marks)	ssment Test	Formative Assessment Test (10 Marks)	End Ser (60 Ma	mester Exams rks)
1. Description	n Questions	1. Assignment	1. 1	Description
<b>2.</b> Formative	Multiple Choice	2. Online Quizzes		Questions
Questions		<b>3.</b> Problem Solving Activities		Choice Questions
Outcomes				
Upon completion	n of the course, t	he students will be able to:		
CO704.1 D	iscuss the fundame	entals of Devices and their Reliability	y .	
CO704.2 E	xplains the fundan	nentals of Packaging Materials, Proc	esses and	Stresses
CO704.3 D	Pescribe the failure	and reliability of optic materials and	l devices.	
CO704.4 Si de	immarize the cha	racteriastion of failure and reliabi	lity of or	ptic materials and
CO704.5 E	xplain the issues a	nd future directions of reliability.		
Text Books				
1. M. Ohring, Relia 1998.	bility and Failure o	f Electronic Materials and Devices, Fi	rst Editior	h, Academic Press,
2. J.W. McPherson	, Reliability Physic	s and Engineering, Second Edition, Sp	oringer, 20	13.

4. J.Ross, Microelectronic Failure Analysis, Sixth Edition, ASTM International, 2011.

#### **Reference Books**

1. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw-Hill, 2002.

#### Web Resources

- 1. https://nptel.ac.in/courses/117/106/117106091/
- 2. https://m.eet.com/media/1120313/ic%20wearout%20edn%20v1-1%20%282%29.pdf
- 3. https://www.sciencedirect.com/book/9780120885749/reliability-and-failure-of-electronicmaterials-and-devices

CO Vs PO Mapping and CO Vs PSO Mapping

CO	PO1	PO2	PO3	PO4	PO5	<b>PO6</b>	<b>PO7</b>	<b>PO8</b>	<b>PO9</b>	<b>PO10</b>	PO11	PO12	PSO1	PSO2	PSO3
1	3	3										3		2	
2	3		3									3			
3				3								3		3	
4	3			3	3	3						3			
5	3			3	3	3	3					3			1
		• • •		2 \ 1											

1→Low 2→Medium 3→High

PROFESSIONAL ELECTIVE II										
21VL1705	Graph Theory and Algorithms for CAD	3	0	0	3					
21VL1706	Communication Buses and Interfaces	3	0	0	3					
21VL1707	Mixed Signal Design	3	0	0	3					
21VL1708	VLSI Architectural Design and Implementation	3	0	0	3					

21VL1705	GRAPH THEORY AND ALGORITHMS FOR CAD	L	Т	Р	C
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Francis Xavier Engi 44

Prerequisites for the course

neering College / Department of ECE	: <i> M.E-VLSI   R2019   Cu</i>	rriculum and Syllabi 2021
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3	0	0

3

The pre-req	uisite knowledge	required by the Students to	o study this Course	is basic knowledge in
	of Design.			
1 To learn gra	nh theory concept	s in VI SI Design		
$\begin{array}{c} 1.  10 \text{ features grade} \\ 2  \text{To study the study of } \end{array}$	ipii theory concept	s III v LSI Desigli.	with proper place	ment and partitioning
2. 10 study u	le designi fuies ai	iu implement the Layout	with proper place	ment and partitioning
3 To learn alo	orithms to perform	n Floor planning		
4 To understa	nd VLSI design a	tomation tools		
5. To study me	delling and simul	ation.		
UNIT I	6	<b>GRAPH THEORY</b>		9
Basic Definitions a Cycles – Vertex Co Formula– Dual Gr Algorithms - Span	and Examples – T plourings – Edge aphs -Data struct ing tree algorithm	rees and their Characteriz Colourings – Vizing's The ures for graph representat s and shortest path algorith	ation – Euler Circu orem – Planar Gra tions – Application nms.	uits – Long Paths and phs –Including Euler's as in CAD for VLSI-
UNIT II	COMPU	JTATIONAL COMPLEX	XITY OF	9
Tractable and Intra notation- Class P- c	actable problems, lass NP -NP-hard	General purpose method - NP-complete.	s for combinatoria	l optimization. Big-O
UNIT III	LAY	OUT AND PARTITION	NING	9
Layout Compaction Problem formulat Partitioning.	n, Design rules, F ion- Group Mig	Problem formulation, Algo ration Algorithm: Kern	orithms for constra ighan-Lin Simula	int graph compaction, ted annealing based
UNIT IV	PIN ASS	SIGNMENT AND PLAC	EMENT	9
<b>Pin Assignment:</b> O <b>Placement:</b> Wire technique	Concentric circle m length estimation	apping, Topological pin as models for placement	ssignment- Power a - Quadratic place	ind ground routing. ment- Sequence pair
UNIT V	SIMULA	TION AND LOGIC SYN	NTHESIS	9
Simulation, Gate-le	vel modelling and	simulation, Switch-level	modelling and simu	lation, Combinational
Logic Synthesis,	Binary Decision	Diagrams, Two Level	Logic Synthesis.	High-level synthesis-
allocation, assignm	nent and schedu	ling, scheduling algorith	nms, Assignment	problem, High level
transformations.				
			<b>Total Periods</b>	45
Suggestive Asses	sment Methods			
Continuous Asses (30 Marks)	ssment Test	Formative Assessmen (10 Marks)	t Test End Se (60 Ma	mester Exams rks)
1. Description	n Questions	1. Assignment	1.	Description
<b>2.</b> Formative	Multiple Choice	2. Online Quizzes		Questions
Questions		<b>3.</b> Problem Solving	Ζ.	Formative Multiple
Outcomes		Activities		
Upon completion	of the course. t	he students will be able	to:	
<u>r</u>			*	

CO705.1 Understand graph theory concepts in VLSI Design.

- CO705.2 Understand the design rules and implement the Layout with proper placement and partitioning algorithm.
- CO705. 3 Learn algorithms to perform Floor planning.
- CO705.4 Learn algorithms for Assignment and placement.
- CO705. 5 Understand the scheduling algorithms Synthesis Simulation process.

## **Text Books**

- 1. Narasingh Deo, Graph Theory with Applications to Engineering and Computer Science, PHI Learning Pvt Ltd, 2004.
- 2. Gerez, Algorithms for VLSI Design Automation, John Wiley & Sons 2000.
- 3. Sadiq M. Sait, Habib Youssef, "VLSI Physical Design automation: Theory and Practice", World Scientific 1999.

### **Reference Books**

1. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002.

Web Resources

- 1. https://nptel.ac.in/courses/106/106/106106088/
- https://gndec.ac.in/~librarian/web%20courses/IIT-MADRAS/CAD%20for%20VLSI%20DESIGN%20I/index1.html

CO Vs PO Mapping and CO Vs PSO Mapping

CO	PO1	PO2	PO3	PO4	PO5	PO6	<b>PO7</b>	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	3	3													
2	3	3											2		
3	3	3													
4	3	2												2	
5	3	2											1		

1→Low 2→Medium 3→High

21VL1706

COMMUNICATION BUSES AND INTERFACES

L	Т	Р	C
3	0	0	3

### Prerequisites for the course

• The pre-requisite knowledge required by the Students to study this Course is basic knowledge in Microcontrollers and Interfacing.

Objectives								
1. Learn to de	esign RS232 based	system.						
2. Understand	the APIs for confi	guration, reading and writing data or	nto serial	bus.				
3. Learn to de	esign peripheral inte	erfaces attached to desired serial bus						
4. To unders	tand the USB arch	itecture						
5. To analyse	e the CAN architec	ture						
UNIT I	LOW SPEE	D SERIAL BUS ARCHITECTUR	RE	9				
Serial Buses RS23	2- I2C- SPI Feature	es- Frame structure- Control signals-	Limitatio	ons.				
UNIT II	LOW SPEED S	SERIAL BUS PHYSICAL INTER	FACE	9				
Serial Bus RS232	2 - physical inter	face; RS485- I2C Physical Interfa	ace - SP	I, Physical Interface;				
Configuration and	applications of low	v speed serial bus.						
UNIT III		CAN ARCHITECTURE		9				
CAN Features -	Architecture; Fran	ne structure - Physical Interface	of CAN	; Data transmission-				
Applications of CA	AN protocol							
UNIT IV		<b>USB ARCHITECTURE</b>		9				
USB Architecture-	-Transfer types; En	umeration; Descriptor types and con	ntents; De	evice driver.				
UNIT V		PCIe ARCHITECTURE		9				
PCIe Architecture	-Revisions- Featur	es; PCIe Configuration space; Hard	dware pro	tocols, Applications				
		Total I	Periods	45				
Suggestive Asses	ssment Methods							
Continuous Asse	essment Test	Formative Assessment Test	End Se	mester Exams				
(30 Marks		(10 Marks)	(60 Ma	rks)				
1. Descriptio	on Questions	1. Assignment	1. 1	Description				
<b>2.</b> Formative	Multiple Choice	2. Online Quizzes	(	Questions				
Questions		<b>3.</b> Problem Solving	<b>2.</b> 1	Formative Multiple				
		Activities		Choice Questions				
Outcomes								
Upon completion	n of the course, t	he students will be able to:						
CO706.1 S	elect Low speed Se	rial buses for various applications.						
CO706.2 D	emonstrate Low sp	eed serial buses Configuration.						
CO706. 3 Ir	nterpret Automotive	e Bus Frame structure.						
CO706.4 A	analyze USB Descri	ptors.						
CO706.5 D	escribe high speed	PCIe bus configuration space.						
Text Books		-						
1. Jan Axelso	n, Jan. USB compl	ete . Lakeview Research, 2015						
2. Mike Jacks	son, Ravi Budruk, "	PCI Express Technology", Mindsha	re Press					
Reference Books	S							
1. Jan Axelso	1. Jan Axelson, J. Serial Port Complete: COM Ports, USB Virtual COM Ports, and Ports for							
Embedded	Systems, ser. 2nd I	Edition, Complete Guides Series. Lal	keview R	esearch 2007.				
2 Wilfried Voss A Comprehensible Guide to Controller Area Network Copperbill Media								
$\angle$ . WINNEU	Voss, A Compreh	ensible Guide to Controller Area	i networ	K, Copperinit Media				
2. Winned Corporatio	Voss, A Compreh $n_{1}^{2nd}$ Edition 2005	ensible Guide to Controller Area	i networ	k, Coppernin Media				
2. Winned Corporatio 3. Serial From	Voss, A Compreh n, 2 <sup>nd</sup> Edition, 2005 at Panel Draft Stand	ensible Guide to Controller Area 5. ard VITA 17.1 – 200x	i Networ	k, Coppernin Media				
2. Willied Corporatio 3. Serial From	Voss, A Compreh n, 2 <sup>nd</sup> Edition, 2005 at Panel Draft Stand	ensible Guide to Controller Area 5. ard VITA 17.1 – 200x. Mao Jeong-dong Pyoe Viber Li "		secontials" Cambridge				

#### University Press.

#### Web Resources

- 1. https://www.usb.org/
- 2. https://www.can-cia.org/

## CO Vs PO Mapping and CO Vs PSO Mapping

CO	PO1	PO2	PO3	PO4	PO5	PO6	<b>PO7</b>	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	3	3												2	
2	2	1	2												
3	3	2											2		
4	1	2												3	
5	2	1											1		
			Andim	m 3-71	High										

#### $1 \rightarrow Low 2 \rightarrow Medium 3 \rightarrow High$

21VL1707	MIXED SIGNAL DESIGN	L	T	Р	С
		3	0	0	3

#### Prerequisites for the course

• The pre-requisite knowledge required by the Students to study this Course is VLSI Design and Embedded systems.

#### Objectives

**UNIT I** 

- 1. To give the knowledge about various analog and digital CMOS circuits
- 2. To impart the skill in analysis and design of analog and digital CMOS circuits.
- 3. To design the amplifiers
- 4. To understand the principle of oscillators
- 5. To analyse the switched capacitor circuits and converters

CMOS AMPLIFIERS AND CASCODED STAGES

**CMOS Amplifiers-** Common Source with diode connected loads and current source load, CS stage with source degeneration, CG stage and Source Follower (Only Voltage Gain and Output impedance of circuits )

**Cascoded stages -** Cascoded amplifier, Cascoded amplifier with cascoded loads , Folded cascode Amplifier

UNIT II	MOS CURRENT MIRROR AND DIFFERENTIAL	9
	AMPLIFIERS	

**MOS Current Mirror**- Basic circuit, PMOS and NMOS current mirrors Current mirror copying circuits, MOSFET cascode current mirror Circuits

**Differential Amplifiers-**Differential Amplifier with MOS current source Load, with cascaded load and with current mirror load, MOS telescopic cascode amplifier. (Only Voltage Gain and Output impedance of circuits)

UNIT III CMOS OP AMPS AND COMPARATOR

9

9

**CMOS OP AMPS-** Two Stage Operational Amplifiers - Frequency compensation of OPAMPS - miller compensation – Design of classical Two Stage OP AMP

Comparator- Characterization of a comparator-static and dynamic, A Two stage open loop comparator

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	UNI	TIV		PHAS	E LOO	CKED	LOO. CII	P ANL RCIII	D D Y N FS	AMIC	ANAL	ÜĞ		9	
Ph	ase La	ocked	Loop -	– Simp	le PLI	Basic	c PLL	Topolo	ogy. Ch	narge Pr	mp PL	L. Basi	c Charge	Pump F	<u>NL</u>
Dy	nami	c analo	og circ	uits –	charge	injecti	on and	l capac	itive fe	ed thro	ugh in N	MOS sv	vitch, Re	duction	
tec	hnique	e	C		U	U		•			U		·		
	UNI	T V		S	WITC	HED	CAPA	CITO	R CIR	CUITS	AND			9	
							CON	VERT	ERS						
Sw	vitched	d Capa	acitor	Circui	ts- san	iple an	d hold	circuit	s, Swit	tched C	apacitor	Integr	ator, Lad	der filte	rs
Da	ita Co	nverte	rs - DA	AC Spe	CIFICAT	ions-D	NL, IN	NL, late	ency, S	NR, Dy	namic I	Range A	ADC Spe	ecificatio	ons-
		tion er	turo	lasing,	SINK,	Aperu a Cho	rao So	or. olina o	nd Din	alina tu	nos				
	AC Ar	chitec	ture - I ture. F	Tlash a	nd Pine	g, Clia line t	nge Sc	anng a	na rip	enne ty	pes.				
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U	munu) ۲)	ous As 30 Mai	rks)	ent re	51	ru.	1 mau v (	10 Ma	rks)	i resi		hu Sel 60 Mar	ks)	xams	
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	2. F	ormati	ve Mu	ltiple (	Choice		2. O	nline Q	uizzes			2. F	Formative	e Multip	le
	Q	uestio	ns	1			<b>3.</b> Pr	oblem	Solvin	ıg		(	Thoice Q	uestions	,
							A	ctivitie	s						
Oı	itcom	es													
UĮ	on co	mpleti	ion of t	the cou	ırse, tl	ne stud	lents v	vill be	able to	):					
	CO7(	07.1	Can ı	underst	and Cl	MOS A	Amplifi	iers and	d Case	oded St	ages				
	CO7(	07.2	Can u	underst	and M	OS Cu	rrent N	Mirror	and Di	fferenti	al Ampl	ifiers			
	CO7(	07.3	Can u	underst	and Cl	MOS (	Dp Am	ps and	Comp	arator					
	CO7(	07.4	Can u	underst	and Ph	ase Lo	ocked I	Loop a	nd Dyr	namic A	nalog C	Circuits			
	CO7(	07.5	Can u	underst	and Sv	vitched	l Capa	citor C	ircuits	and Co	nverters	5			
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3.	Behza	d Raza	vi, "De	esign o	f Anal	og CM	IOS In	tegrate	d Circu	uits", M	cGraw	Hill, 20	00		
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1.	Baker,	, Li, Bo	oyce, C	CMOS:	Circui	ts Des	ign, La	yout a	nd Sin	nulation	, Prentic	e Hall	India, 20	000	
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Francis Xavier Engineering College | Department of ECE |M.E-VLSI | R2019 | Curriculum and Syllabi 2021 49 2 3 1 3 2 3 2 2 3 2 4 3 3 2 5 2 1  $1 \rightarrow Low 2 \rightarrow Medium 3 \rightarrow High$ 21VL1708 VLSI ARCHITECTURAL DESIGN AND L Т Р С **IMPLEMENTATION** 3 0 3 0 Prerequisites for the course The pre-requisite knowledge required by the Students to study this Course is basic knowledge in CMOS VLSI Design. **Objectives** 1. To review the architectural design of VLSI systems as seen in complex SoCs. 2. To learn performance optimization techniques in VLSI signal processing. 3. To understand the design of synchronous clocking and flow of asynchronous data processing. 4. To understand the VLSI circuit floorplan and chip assembly. 5. To understand the physical design and verification **INTRODUCTION TO VLSI ARCHITECTURE UNIT I** 9 Introduction: Review of VLSI Design flow. Goals of VLSI Design: Optimization of speed, power dissipation, cost and reliability - Algorithm to architecture transformation: Architectural antipodes, transform approach to VLSI architectures, graph based formalism for describing processing algorithms, isomorphic architecture - Equivalence transforms for combinational computations: Common assumptions, pipelining, replication, time sharing, associatively transform and other algebraic transforms **ARCHITECTURAL SYNTHESIS AND** 9 **UNIT II OPTIMIZATION** Architectural Synthesis and Optimization: Circuit specifications for architectural synthesis, fundamental architectural synthesis problems, temporal domain-scheduling, spatial domain binding, sequencing graphs, hierarchical models, synchronization problem, area and performance estimation, data path and control unit synthesis, constrained and unconstrained scheduling, scheduling of pipelined circuits **UNIT III DESIGN & CLOCKING OF SYNCHRONOUS** 9 **CIRCUITS** The grand alternatives for regulating state changes - Why a rigorous approach to clocking is essential in VLSI -The dos and don'ts of synchronous circuit design - Clocking of Synchronous Circuits: difficulty in clock distribution - skew and jitter within tight bounds - Input/output timing - Clock gating properly **ASYNCHRONOUS DATA PROCESSING** 9 **UNIT IV** ARCHITECTURES Data consistency problem of vectored acquisition-plain bit parallel synchronization, Unit distance coding, Suppression of cross patterns, handshaking, partial handshaking, Data consistency problem of scalar acquisitionsynchronization at single place, Synchronization at multiple places, Synchronization from a slow clock, Metastable synchronizer behaviour- Energy Efficiency and Heat Removal: Energy dissipated in CMOS circuits -How to improve energy efficiency - Heat flow and heat removal **UNIT V PHYSICAL DESIGN & VERIFICATION** 9 Conducting layers and their characteristics - Cell-based back-end design - Floorplanning -Identify major building blocks and clock domains - Establish a pin budget- Find a relative arrangement of all major building blocks - Plan power, clock, and signal distribution - Place and route (P&R) - Chip assembly

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2. Behrooz Parhami, " Computer Arithmetic: Algorithm and Hardware Design", Behrooz Parhami,																		
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#### Prerequisites for the course

• Analog and Digital IC

## Objectives

- 1. To familiarize various representation methods of DSP algorithms, understand the significance of the iteration bound and to calculate the same for a given single-rate and/or multi-rate DFG.
- 2. To understand retiming and pipelining and parallel processing.

Computation, Rounding Noise in Pipelined IIR Filters.

- 3. To understand algorithms unfolding and folding on a given DFG.
- 4. To understand the concepts of fast convolution, pipelining and parallel processing for FIR and IIR filters
- 5. To signify and calculate the effects of numerical strength reduction, scaling and round-off noise for a given digital filter with limited word length.

UNIT I	INTRODUCTION TO SIGNAL PROCESSING	9
Typical DSP Al	gorithms – DSP Application Demands and Scaled CM	OS Technologies -
Representations of	DSP Algorithms - Data-Flow Graph Representations. Introduct	tion -Loop Bound and
Iteration Bound -A	lgorithms for Computing Iteration Bound: Longest Path Matri	x and Multiple Cycle
Mean algorithms -	Iteration Bound of Multi-rate Data Flow Graphs.	
UNIT II	PIPELINING, PARALLEL PROCESSING AND	9
	RETIMING	
Pipelining, Paralle	l processing and Retiming- Introduction to Retiming -Definit	ions and Properties -
Solving Systems	of Inequalities - The Bellman-Ford Algorithm - The Floyd	Warshall Algorithm-
Retiming Techniqu	es.	
UNIT III	UNFOLDING AND FOLDING	9
Introduction, An	Algorithm for Unfolding, Properties of Unfolding, Critical	Path, Unfolding, and
Retiming, Applica	tions of Unfolding, Introduction, Folding Transformation, F	Register Minimization
Techniques, Regist	er Minimization in Folded Architectures.	-
UNIT IV	FAST CONVOLUTION, PIPELINING AND	9
	PARALLEL PROCESSING FOR FIR AND IIR	
	FILTERS	
Fast convolution -	- Cook-Toom algorithm, modified Cook-Toom algorithm, F	ripelined and parallel
recursive filters –	Look-Ahead pipelining in first-order IIR filters, Look-Ahead p	ipelining with power-
of-2 decompositio	n, Clustered look-ahead pipelining, Parallel processing of	IR filters, combined
pipelining and para	llel processing of IIR filters.	
UNIT V	NUMERICAL STRENGTH REDUCTION, SCALING	9
	AND ROUNDING NOISE	
Introduction, Nume	erical strength reduction - subexpression elimination, multiple co	onstant multiplication,
Scaling and Round	ing Noise, State Variable Description of Digital Filters, Scaling	and Rounding Noise

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CO701.	3 Apply	y unfolding an	d foldin	g on the given	DFG.				
CO701.	4 Under filters	rstand concep	ts of fast	convolution,	pipelining and	parallel proc	cessing for FII	R and IIR	Ł
CO701.	5 Under scalin	rstand and app og and round-o	oly algor	of the given of	merical strength ligital filter with	n reduction 1 n limited wo	methods and c ord length.	calculate	
Text Books	5				. ~			_	
1. Kesh	ab K. Par	hi, VLSI	Digital	Signal Pro	cessing System	ems: Desi	ign and Imp	olementa	ation,
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3. Moh	ammed Is	smail and Te	erri Fiez	Analog VI	SI Signal and	l Informati	on Processir	ng. McC	iraw-
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4. S.Y.	Kung, H.	J. White Hou	ise, T. F	Kailath, VLS	and Modern	Signal Proc	cessing, PHI,	2010.	
5. S. K	. Mitra, l	Digital Signa	l Proces	ssing –A Cor	mputer Based	Approach,	Fourth Edition	on, McC	Braw-
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CC CC CC	702.2	CO702. 2 Understand scripting languages												
CC CC		Unde	rstand	l securi	ity issu	ies								
CC	702.3	Expla	ain con	cept of	f TCL p	ohenor	mena							
	0702.4	Expla	ain adv	vanced	TCL	_								
CC	0702.5	Discu	iss TK	and Ja	iva scri	ipt								
Text B	Fext Books													
1.Bren	t Welch,	"Practi	cal Pro	)gramn	ning in	Tcl ar	nd Tk", "	Fourth	Edition	n, 2003.	000			
2. Dav: $2 \cdot 1 \cdot 1$	id Barro	n, "The	Work	1 of Sc	rıptıng	Langu	iages",	Wiley	Publica	ations, 2	000.			
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#### Prerequisites for the course

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CMOS VLSI Design
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#### **Objectives**

- 1. Expounding the basics and detailed architecture of SRAMs and DRAMs.
- 2. Model the memory fault and introduce the basic and advanced memory testing patterns.
- 3. To get an overview on reliability of semiconductors.
- 4. Review and discuss high performance memory subsystems, advanced memory technologies and contemporary issues.
- 5. To understand the advanced memory technologies
- **RANDOM ACCESS MEMORY TECHNOLOGIES UNIT I**

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SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit Operation, Bipolar SRAM Technologies-Silicon On Insulator (SOI) Technology Operation, Advanced SRAM Architectures and Technologies-Application Specific SRAMs, DRAM Technology Development-CMOS DRAMs, DRAMs Cell Theory and Advanced Cell Strucutures - BiCMOS, DRAMs, Soft Error Failures in DRAMs, Advanced DRAM Designs and Architecture-Application Specific DRAMs

UNIT II	NONVOLATILE MEMORIES	9
Masked Read-Only	y Memories (ROMs) - High Density ROMs, Programmable	Read-Only Memories
(PROMs) - Bipola	arPROMs-CMOS PROMs, Erasable (UV) - Programmable	Road-Only Memories
(EPROMs) - Floati	ng-Gate EPROM Cell-One-Time Programmable (OTP) Eproms	- Electrically Erasable
PROMs (EEPROM	As)-EEPROM Technology And Architecture, Nonvolatile SR.	AM, Flash Memories

(EPROMs or EEPROM), Advanced Flash Memory Architecture.

MEMORY FAULT MODELING AND TESTING **UNIT III** 

RAM Fault Modelling, Electrical Testing, Peusdo Random Testing-Megabit DRAM Testing, Nonvolatile Memory Modelling and Testing, IDDQ Fault Modelling and Testing, Application Specific Memory Testing

UNIT IV	SEMICONDUCTOR MEMORY RELIABILITY	

General Reliability Issues, RAM Failure Modes and Mechanism, Non-volatile Memory Reliability, Reliability Modelling and Failure Rate Prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and Qualification.

UNIT V **ADVANCED MEMORY TECHNOLOGIES** 9 Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories-Magneto-resistive Random Access Memories (MRAMs), Experimental Memory Devices. Memory Hybrids and MCMs (2D) - Memory Stacks and MCMs (3D), Memory MCM Testing and Reliability Issues, Memory Cards, High Density Memory Packaging Future Directions.

	Total	Periods	45
Suggestive Assessment Methods			
<b>Continuous Assessment Test</b>	Formative Assessment Test	End Se	mester Exams
(30 Marks)	(10 Marks)	(60 Ma	rks)
1. Description Questions	1. Assignment	1. l	Description
<b>2.</b> Formative Multiple Choice	2. Online Quizzes	(	Questions
Questions	3. Problem Solving	2. 1	Formative Multiple
	Activities	(	Choice Questions
Outcomes			

Upon completion of the course, the students will be able to:

- CO703.1 Design SRAMs and DRAMs.
- CO703. 2 Design NVRAMs and Flash Memories..
- CO703.3 Model memory faults, select suitable testing patterns and develop testing patterns.
- CO703.4 Improve the reliability of semiconductor memories.
- CO703.5 Contribute to the development of high performance memory subsystems and use advanced memory technologies.

#### **Text Books**

- 1. Ashok K. Sharma, "Semiconductor Memories: Technology Testing and Reliability" Prentice Hall of India", 2007.
- 2. Ashok K. Sharma, "Semiconductor Memories Two Volume Set", Wiley, IEEE Press 2003.

### **Reference Books**

- 1. Brent Keeth, R. Jacob Baker, Brian Johnson, Freng Lin, "DRAM Circuit Design: Fundamental and High Speed Topics", Wiley-IEEE Press, Second Edition, 2008
- 2. Brent Keeth, R. Jacob Baker, "DRAM Circuit Design: A Tutorial", Wiley, IEEE Press, 2000
- 3. Betty Prince, "Emerging Memories Technologies and Trends", Kluwer Academic Publishers, 2002.

#### Web Resources

- 1. Memory Technology, https://www.sciencedirect.com/topics/computer-science/memorytechnology
- 2. Reliability of Semiconductor Memories from a Practical Point of View, https://link.springer.com/chapter/10.1007%2F978-3-322-83629-8\_22
- 3. Advanced memory—Materials for a new era of information technology, https://doi.org/10.1557/mrs.2018.96

## CO Vs PO Mapping and CO Vs PSO Mapping

CO	PO1	PO2	PO3	PO4	PO5	PO6	<b>PO7</b>	PO8	<b>PO9</b>	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	3	2												3	
2	2	2	3											2	
3	2	3	2											1	
4	1	1													1
5	2	3	1												2
		• > -													

 $1 \rightarrow Low 2 \rightarrow Medium 3 \rightarrow High$ 

Francis Xavier Engineering College | Department of ECE |M.E-VLSI | R2019 | Curriculum and Syllabi 2021 57 SYSTEMS ON CHIP DESIGN 21VL2704 L Т Р С 3 3 0 0 Prerequisites for the course 1. Digital electronics 2. System architecture **Objectives** 1. To understand concept of Systems-on-Chip 2. To implement SoC on processors. 3. To obtain skills to design SoC using ADL. 4. To develop skills in applying SoC for real time applications 5. To understand the no instruction set computer UNIT I **INTRODUCTION TO SoC DESIGN** 9 Architecture of the Present Day SoC-Design Issues of SoC-Hardware Software Codesign-SoC Design Flow-General Guidelines for Design Reuse-Synchronous Design-Memory and Mixed-Signal Design-On-Chip Buses-Clock Distribution-Clear/Set/Reset Signals-Physical Design-Design Process for Soft and Firm Cores-System Integration-Designing With Hard Cores-Designing With Soft Cores **UNIT II** PROCESSORS FOR SoC 9 Processor Selection for SOC-Basic Concepts in Processor Architecture-Basic Concepts in Processor Microarchitecture-Basic Elements in Instruction Handling-Buffers: Minimizing Pipeline Delays-VLIW Processors-Superscalar Processors-Processor Evolution SoC MEMORY AND INTERCONNECT DESIGN **UNIT III** 9 Overview-Scratchpads and Cache Memory-Basic Notion-Cache Organization-Cache Data-Write Policies-Strategies for Line Replacement at Miss Time-Multilevel Caches-SOC (On-Die) Memory Systems-Simple DRAM and the Memory Array-Models of Simple Processor-Memory Interactions-Overview: Interconnect Architectures-Bus: Basic Architecture-SOC Standard Buses **UNIT IV** ADL AND NISC 9 Architecture Description Languages (ADL) for design and verification of Application Specific Instruction set Processors (ASIP), No-Instruction-Set-computer (NISC) - design flow, modeling NISC architectures and systems, use of Generic Netlist Representation - A formal language for specification, compilation and synthesis of embedded processors. UNIT V **SoC APPLICATION STUDY** 9 SOC Design Approach,-AES-3-D Graphics Processors-Image Compression-Video Compression-Further Application Studies-Challenges Ahead-Overview-Powering the ASOC-The Shape of the ASOC-Computer Module and Memory-RF or Light Communications-Pre-Deployment-Post-Deployment **Total Periods** 45 Suggestive Assessment Methods **Continuous Assessment Test Formative Assessment Test End Semester Exams** (30 Marks) (10 Marks) (60 Marks) 1. Description 1. Description Questions 1. Assignment 2. Formative Multiple Choice 2. Online Quizzes Questions Questions **3.** Problem Solving **2.** Formative Multiple Activities **Choice Questions** 

#### Outcomes

#### Upon completion of the course, the students will be able to:

CO704.1 To understand the concept of SoC and its design flow

- CO704.2 To learn and understand implementation of SoC on different processors.
- CO704.3 To learn and understand the memory design and interconnection architecture in SoC
- CO704.4 To learn and implement fault tolerance and monitoring services on NOC

CO704. 5 To apply the SoC concept for various eal time applications.

#### **Text Books**

- 1. RochitRajsuman, "System-on- a-chip: Design and test", Advantest America R & D center, 2000.
- 2. P Mishra and N Dutt, "Processor Description Languages", Morgan Kaufmann, 2008
- 3. Michael J. Flynn and Wayne Luk, "Computer System Design: System-on-Chip". Wiley, 2011.

#### **Reference Books**

- 1. Hubert Kaeslin, "Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication", Cambridge University Press, 2008.
- 2. B. Al Hashimi, "System on chip-Next generation electronics", The IET, 2006

#### Web Resources

- 1. https://www.cerc.utexas.edu/~jaa/soc/lectures/1-2.pdf
- 2. https://www.cl.cam.ac.uk/teaching/1516/SysOnChip/materials.d/socdam-notes00.pdf
- 3. https://nptel.ac.in/courses/108102045/10

## CO Vs PO Mapping and CO Vs PSO Mapping

СО	PO1	PO2	PO3	PO4	PO5	PO6	<b>PO7</b>	PO8	<b>PO9</b>	PO10	PO11	PO12	PSO1	PSO2	PSO3
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## 1→Low 2→Medium 3→High

PROFESSIONAL	LELECTIVE IV				
21VL2705	VLSI Test and Testability	3	0	0	3
21VL2706	VLSI Digital Design Verification	3	0	0	3
21VL2707	Modern Computer Architecture	3	0	0	3
21VL2708	Electronic Design Automation	3	0	0	3

21VL2705	VLSI TEST AND TESTABILITY	L	Τ	Р	С
		3	0	0	3
<b>Prerequisites for</b>	the course				

• The pre-requisite knowledge required by the Students to study this Course is basic knowledge in Digital Design and CMOS VLSI DESIGN

#### **Objectives**

- 1. To Identify the significance of testable design
- 2. To Generate optimized test patterns for combinational and sequential logic circuits
- 3. To Enables to design for testability
- 4. To Design scan chains and BIST modules for digital designs
- 5. To Understand boundary scan based test architectures

UNIT I

#### **BASICS OF TEST**

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Design and Test, Test Concerns, HDLs in Digital System Test, ATE Architecture and Instrumentation, Challenges in VLSI Testing, Levels of Abstraction in VLSI Testing, Historical Review of VLSI Test Technology, Fault Modeling, Structural Gate Level Faults, Issues Related to Gate Level Faults, Fault Collapsing

UNIT II	TEST PATTERN GENERATION METHODS AND	
	ALGORITHMS	

Test Generation Basics, Controllability and Observability, Random Test Generation, Designing a Stuck-At ATPG for Combinational Circuits, Reed –Muller Expansion Technique, Designing a Sequential ATPG

UNIT III	

#### **DESIGN FOR TESTABILITY**

Design for Testability Basics, Scan Cell Designs, Scan Architectures, Scan Design Rules, Scan Design Flow, Special-Purpose Scan Designs, Fault Simulation, Combinational Logic Diagnosis, Scan Chain Diagnosis

UNIT IV

**BUILT-IN SELF-TEST** 

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BIST Design Rules, Test Pattern Generation, Output Response Analysis, Logic BIST Architectures, Digital Boundary Scan, Boundary Scan for Advanced Networks, Embedded Core Test Standard, IDDQ Testing, Logic BIST Diagnosis

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	CO7	05.1	To Id	lentify	the sign	nifican	ce of te	estable	design						
	CO7	05.2	To G	lenerate	e optin	nized to	est patt	terns fo	or com	oination	al and s	equentia	al logic o	circuits	
	CO7	05.3	To E	nables	to desi	ign for	testab	ility							
	CO7	05.4	To D	esign s	scan ch	ains ai	nd BIS	T mod	ules fo	r digital	design	s			
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21VL2706	VLSI DIGITAL DESIGN VERIFICATION	L	Т	Р	(
		-			2
Prerequisites fo	or the course	3	U	U	3
• The pre-re	equisite knowledge required by the Students to study this Course	is ba	sic kn	owled	lge
Digital De	esign and VLSI DESIGN.	15 0 0			-8-
Obiectives					
1. To introdu	ace various verification techniques				
2. To Discus	s the principle and importance of verification				
3. To Develo	p basic verification environment using System Verilog				
4. To Develo	p self-checking test environment				
5. To Create	random stimulus and track functional coverage using System Ver	rilog			
UNIT I	VERIFICATION CONCEPTS AND DATA TYPES			9	
The Verification	Process- Basic Testbench Functionality, Directed Testing,	Con	strain	ed-Ra	ndc
Stimulus, Function	nal Coverage, Testbench Components, Built-In Data Types, Fixed	d-Size	e Arra	ays,Qu	ieue
$\Delta$ ssociative $\Delta$ rray	a Amore Matheda Streaming Operators Environmented Types				
	s, Array Methods, Streaming Operators, Enumerated Types				
UNIT II	SYSTEMVERILOG PROCEDURAL BLOCKS, TASKS AND FUNCTIONS			9	
UNIT II Verilog general	SYSTEMVERILOG PROCEDURAL BLOCKS, TASKS AND FUNCTIONS purpose always procedural block, System Verilog specialize	ed pr	ocedu	9 ural bl	locl
UNIT II Verilog general Enhancements to	SYSTEMVERILOG PROCEDURAL BLOCKS, TASKS AND FUNCTIONS purpose always procedural block, System Verilog specialize tasks and functions, Task and Function Overview, Routine Argus	ed prometer	ocedu	<b>9</b> Iral bl	locl fro
UNIT II Verilog general Enhancements to a Routine, Local	SYSTEMVERILOG PROCEDURAL BLOCKS, TASKS AND FUNCTIONS purpose always procedural block, System Verilog specialize tasks and functions, Task and Function Overview, Routine Argun Data Storage, Time Values	ed prometer	ocedu s, Retu	<b>9</b> Iral bl Irning	locl frc
UNIT II Verilog general Enhancements to a Routine, Local	SYSTEMVERILOG PROCEDURAL BLOCKS, TASKS AND FUNCTIONS purpose always procedural block, System Verilog specialize tasks and functions, Task and Function Overview, Routine Argun Data Storage, Time Values TESTBENCH AND DESIGN	ed prometer	ocedu s, Retu	9 Iral bl Irning 9	loc] fro
UNIT II Verilog general Enhancements to a Routine, Local UNIT III Separating the Te	Systemining Operators, Enumerated Types         SYSTEMVERILOG PROCEDURAL BLOCKS, TASKS AND FUNCTIONS         purpose always procedural block, System Verilog specialize tasks and functions, Task and Function Overview, Routine Argun Data Storage, Time Values         TESTBENCH AND DESIGN         testbench and Design, The Interface Construct, Stimulus Timing,	ed prometers	ocedu s, Retu face I	9 Iral bl Irning 9 Drivin	locl frc
UNIT II Verilog general Enhancements to a Routine, Local UNIT III Separating the Te Sampling, Progra	Systemations, Streaming Operators, Enumerated Types         SYSTEMVERILOG PROCEDURAL BLOCKS, TASKS AND FUNCTIONS         purpose always procedural block, System Verilog specialize tasks and functions, Task and Function Overview, Routine Argun Data Storage, Time Values         TESTBENCH AND DESIGN         estbench and Design, The Interface Construct, Stimulus Timing, am Block Considerations, System Verilog Assertions, The Fo	ed proments ments Inter ur-Po	ocedu s, Retu face I rt AJ	9 ural bl urning 9 Drivin	loci fro
UNIT II Verilog general Enhancements to a Routine, Local I UNIT III Separating the To Sampling, Progra	System Methods, Streaming Operators, Enumerated Types         SYSTEMVERILOG PROCEDURAL BLOCKS, TASKS AND FUNCTIONS         purpose always procedural block, System Verilog specialized tasks and functions, Task and Function Overview, Routine Argun Data Storage, Time Values         TESTBENCH AND DESIGN         estbench and Design, The Interface Construct, Stimulus Timing, am Block Considerations, System Verilog Assertions, The Fo         nization Problems, Atomic Stimulus Generation vs. Scenario Generation	ed proments ments Inter ur-Po eratio	ocedu s, Retu face I rt A7 n	9 ural bl urning 9 Drivin	locl frc g an oute
UNIT II Verilog general Enhancements to a Routine, Local I UNIT III Separating the To Sampling, Progra Common Randor	Systemating Operators, Enumerated Types         SYSTEMVERILOG PROCEDURAL BLOCKS, TASKS AND FUNCTIONS         purpose always procedural block, System Verilog specialize tasks and functions, Task and Function Overview, Routine Argun Data Storage, Time Values         TESTBENCH AND DESIGN         estbench and Design, The Interface Construct, Stimulus Timing, am Block Considerations, System Verilog Assertions, The Fo         nization Problems, Atomic Stimulus Generation vs. Scenario Generation         THREADS AND INTERPROCESS	ed proments ments Inter ur-Po eratio	ocedu s, Retu face I rt AT n	9 aral bl arning 9 Drivin TM R	loc fro
UNIT II Verilog general Enhancements to a Routine, Local UNIT III Separating the To Sampling, Progra Common Randor	System Wethods, Streaming Operators, Enumerated Types         SYSTEMVERILOG PROCEDURAL BLOCKS, TASKS AND FUNCTIONS         purpose always procedural block, System Verilog specialize tasks and functions, Task and Function Overview, Routine Argundata Storage, Time Values         TESTBENCH AND DESIGN         considerations, System Verilog Assertions, The Fo         minuteration Problems, Atomic Stimulus Generation vs. Scenario Generation         THREADS AND INTERPROCESS COMMUNICATION	ed proments ments Inter ur-Po eratio	ocedu s, Retu face I rt AT n	9 Iral bl urning 9 Drivin TM R 9	locl fro g a: out
UNIT II Verilog general Enhancements to a Routine, Local I UNIT III Separating the Te Sampling, Progra Common Randor UNIT IV Working with	System Wethods, Streaming Operators, Enumerated Types         SYSTEMVERILOG PROCEDURAL BLOCKS, TASKS AND FUNCTIONS         purpose always procedural block, System Verilog specialize tasks and functions, Task and Function Overview, Routine Argundata Storage, Time Values         TESTBENCH AND DESIGN         Data Storage, Time Values         TESTBENCH AND DESIGN         estbench and Design, The Interface Construct, Stimulus Timing, am Block Considerations, System Verilog Assertions, The Fo nization Problems, Atomic Stimulus Generation vs. Scenario Gene COMMUNICATION         THREADS AND INTERPROCESS COMMUNICATION         Threads, Disabling Threads, Interprocess Communication,	ed proments ments Inter ur-Po eratio	ocedu s, Retu face I rt AT n	9 rral bl urning 9 Drivin CM R 9 9 Mailb	locl frc g a out
UNIT II Verilog general Enhancements to a Routine, Local I UNIT III Separating the Te Sampling, Progra Common Randor UNIT IV Working with Semaphores, Buil	System Methods, Streaming Operators, Enumerated Types         SYSTEMVERILOG PROCEDURAL BLOCKS, TASKS AND FUNCTIONS         purpose always procedural block, System Verilog specialized tasks and functions, Task and Function Overview, Routine Argundata Storage, Time Values         TESTBENCH AND DESIGN         construct, Stimulus Timing, am Block Considerations, System Verilog Assertions, The Fonization Problems, Atomic Stimulus Generation vs. Scenario Generation Problems, Atomic Stimulus Generation vs. Scenario Generation Problems, Disabling Threads, Interprocess Communication, ding a Testbench with Threads and IPC.	ed proments	ocedu s, Retu face I rt AT n	9 ural bl urning 9 Drivin, TM R 9 9 Mailb	g a out
UNIT II Verilog general Enhancements to a Routine, Local I UNIT III Separating the To Sampling, Progra Common Randor UNIT IV Working with Semaphores, Buil	System Methods, Streaming Operators, Enumerated Types         SYSTEMVERILOG PROCEDURAL BLOCKS, TASKS AND FUNCTIONS         purpose always procedural block, System Verilog specialized tasks and functions, Task and Function Overview, Routine Argundata Storage, Time Values         TESTBENCH AND DESIGN         Data Storage, Time Values         TESTBENCH AND DESIGN         estbench and Design, The Interface Construct, Stimulus Timing, am Block Considerations, System Verilog Assertions, The Fonization Problems, Atomic Stimulus Generation vs. Scenario Generation Problems, Disabling Threads, Interprocess Communication, ding a Testbench with Threads and IPC.         FUNCTIONAL COVERAGE	ed proments ments Inter ur-Po eratio	ocedu s, Retu face I rt AT n	9 ural bl urning 9 Drivin CM R 9 Mailt 9	g a out
UNIT II Verilog general Enhancements to a Routine, Local 1 UNIT III Separating the To Sampling, Progra Common Randor UNIT IV Working with Semaphores, Buil UNIT V Gathering Covera	System in the procedural process in the process in th	ed proments	ocedu s, Retu face I rt AT n ents,	9 rral bl urning 9 Drivin TM R 9 9 Mailb 9 ver Gr	locl frc g a: out
UNIT II         UNIT II         Enhancements to         a Routine, Local 2         UNIT III         Separating the Te         Sampling, Progra         Common Randor         UNIT IV         Working with         Semaphores, Buil         UNIT V         Gathering Covera         Triggering a Covera	Systemmed Systemmed Systemmed Types         Systemverilog PROCEDURAL BLOCKS, TASKS AND FUNCTIONS         purpose always procedural block, System Verilog specialize tasks and functions, Task and Function Overview, Routine Argun Data Storage, Time Values         TESTBENCH AND DESIGN         estbench and Design, The Interface Construct, Stimulus Timing, am Block Considerations, System Verilog Assertions, The Fonization Problems, Atomic Stimulus Generation vs. Scenario Generation Problems, Atomic Stimulus Generation vs. Scenario Generation and Threads, Disabling Threads, Interprocess Communication, ding a Testbench with Threads and IPC.         FUNCTIONAL COVERAGE         ge Data, Coverage Types, Functional Coverage Strategies, Anatomer Group, Data Sampling, Cross Coverage, Generic Cover Groups age Data, Measuring Coverage Statistics During Simulation	ed proments ments Inter ur-Po eratio Eve Eve	face I face I rt AT n ents,	9 rral bl arning 9 Drivin, TM R 9 Mailb 9 ver Gr Optio	g a out

Sı	iggest	ive As	sessn	ient M	ethod	s									
Co	ontinu	ous A	ssessi	ment 7	ſest	Fo	rmati	ve Ass	essm	ent Tes	t E	nd Sem	ester E	Exams	
	(3	0 <u>Mai</u>	rks)				(1	1 <u>0 Ma</u>	r <u>ks)</u>		((	6 <u>0 Mar</u>	ks)		
	1. D	escrip	tion Q	uestio	ns		1. As	ssignm	nent			1. D	escripti	on	
	<b>2.</b> F	ormat	ive Mu	ultiple	Choice	e	2. 0	nline Ç	)uizze:	S		Q	uestion	S	
	Q	uestic	ons				<b>3.</b> Pi	roblem	n Solvi	ng		<b>2.</b> Fo	ormativ	e Multi	ole
							A	ctivitie	es			Cl	noice Q	uestion	5
0	utcom	es								-					
<b>U</b> ]	pon co	omple	tion o	f the c	ourse,	, the st	tuden	ts will	l be at	ole to:					
	CO7	06.1	Intro	oduce v	/arious	s verifi	catior	n techn	iques						
	CO7	06.2	Disc	uss the	princ	iple an	ıd imp	ortanc	ce of v	erificati	on				
	CO7	06.3	Deve	elop bas	sic veri	ificatio	n envi	ronme	nt usin	g Systei	n Verilo	og.			
	CO7	06.4	Deve	elop se	lf-chec	king te	est env	vironme	ent						
	CO7	06.5	Crea	te rand	om stir	nulus a	and tra	ck fun	ctional	coverag	ge using	System	Verilog	g	
T	ext Bo	oks													
	1. C	Thris Sp	pear, C	breogor	y J Tu	mbush	, "Syst	tem Ve	rilog f	or Verif	ication	– A guio	le to lea	rning	
	te	est ben	ch lang	guage f	eatures	s", Spr	inger, i	2012							
	2. S	tuart S	Sutherl	and, S	imon I	Davidn	nann,	Peter I	Flake,	"Systen	n Verilo	og for I	Design -	- A gui	de to
	u	sing S	vstem	Verilo	g for l	nardwa	re des	sign an	d mod	eling",	Springe	r Public	cations,	2nd Ed	ition,
	2	006.	5		0			0			1 0				,
R	eferen	ce Bo	oks												
	1. S	asan I	man, "	Step b	v Step	Functi	ional \	Verifica	ation v	vith Svs	tem Ve	rilog an	d OVM'	'. Hanse	n
	В	rown	Publis	shing, 2	2008.		01							)	
	2. Ja	anick I	Bergero	on "W	riting 7	Festber	iches i	using S	ystem	Verilog	" Synop	osys Inc	., Sprin	ger	
	Р	ublicat	tions, 2	2006.							-	-	-	_	
W	eb Re	sourc	es												
	1. w	/ww.as	sic-woi	rld.											
	2. w	/ww.te	stbenc	h.in											
<u></u>		Manni	ngand	$1 \cap V_{c}$	י חכט א	Ionnir	• ~								
LU	85501	марри	lig and		100	Ларрп	lg								
CO	<b>PO1</b>	<b>PO2</b>	PO3	PO4	PO5	<b>PO6</b>	<b>PO7</b>	<b>PO8</b>	<b>PO9</b>	<b>PO10</b>	PO11	PO12	PSO1	PSO2	PSO3
1	3	3													1
2	2	2	2											2	2
3	3	3	3												
4	1													1	
5	2	1													2
	1→Lov	w 2→N	Mediu	m 3→I	High										
		/ 1			8										

				-			
21VL2707	MODER	N COMPUTER ARCHITECTUR	E	L	Т	Р	С
				3	0	0	3
Prerequisites for	the course			1			4
• The pre-req	uisite knowledge r	required by the Students to study Cor	nputer O	rganiz	ation	Cour	se
Objectives							
1. To provide	broad and deep kn	owledge of computer architecture iss	sues and t	echnic	ques.		
2. Advanced h	ardware-based tec	hniques for exploiting instruction lev	vel paralle	elism.			
3. Knowledge	of various archite	ecture and techniques used for build	ing High	perfo	rman	ce sca	alable
Multithread	ed and Multiproce	ssor system.					
4. Understand	Memory Hierarch	y and Storage System.					
5. Understand	the instruction lev	el parallelism					
UNIT I	FUNDAME	NTALS OF COMPUTER DESIG	N			9	
Pipelining Basics, I	Major Hurdles of F	Pipelining, Overview of Instruction S	et: Archi	tecture	e and		
Operations, Differe Power of IC and Co	nt classes of Compost.	puters, Definition: Computer Archite	ecture, Tr	ends ii	n Tec	hnolo	gy,
UNIT II	INSTRUCT	TION LEVEL PARALLELISM (II	LP)			9	
Algorithm and Exa Multiple Issue.	mples, Statistic Sc	heduling, Exploiting ILP using Dyna	amic, Stat	tistic S	Sched	Hazar uling	and
UNIT III		LIMITATION ON ILP				9	
Introduction, Limit Speculations, Multi	ations on ILP for I ithreading: Thread	Realization Processor, Crosscutting Is -Level Parallelism.	ssues: Ha	rdwar	e and	Softv	vare
UNIT IV	MULTIPR	OCESSOR AND THREAD-LEVE PARALLELISM	EL			9	
Introduction, Symm	netric Shared-Men	norv Architecture. Distributed Shared	d Memor	v and [	Direc	torv-	Based
Coherence, Basics	of Synchronization	n and Models for Memory Consisten	cy.	,		j	
UNIT V	MEN	<b>10RY HIERARCHY DESIGN</b>				9	
Introduction, Optin Crosscutting issues	nization in Cache F in Design of Mem	Performance, SRAM and DRAM, Vinory Hierarchies.	rtual Mei	mory a	und M	Iachir	ies,
		Total F	Periods		4	ł5	
Suggestive Asses	sment Methods						
Continuous Asse (30 Marks)	ssment Test	Formative Assessment Test (10 Marks)	End Se (60 Ma	Semester Exams Marks)			
1. Description	1 Questions	1. Assignment	1. Description				
<b>2.</b> Formative	Multiple Choice	2. Online Quizzes		Questi	ions		
Questions		<b>3.</b> Problem Solving	2.	Forma	ative	Multi	ple
		Activities		Lh01C6	e Que	estion	S

#### **Outcomes**

#### Upon completion of the course, the students will be able to:

- CO707.1 Have broad understanding of the design of computer systems, including modern architectures and alternatives
- CO707.2 Be able to understand Instruction Level Parallelism at Hardware level.
- CO707.3 Be able to understand the limitations of Instruction Level Parallelism at Hardware level.
- CO707.4 Have knowledge of Multiprocessor and Thread-Level Parallelism
- CO707.5 Be able to visualize the Memory structure

#### **Text Books**

- 1. Kai Hwang, "Advanced Computer Architecture", McGraw Hill Education, 1993.
- 2. Kai Hwang, Faye A. Briggs, "Computer Architecture and Parallel Processing" McGrawHill Education. 2012.

#### **Reference Books**

- 1. William Stallings, "Computer Organization and Architecture, Designing for Performance", Prentice Hall, 6th edition, 2006.
- 2. Kai Hwang, "Scalable Parallel Computing", McGraw Hill Education, 1998.
- 3. Harold S. Stone "High-Performance Computer Architecture", Addison-Wesley, 1993.

#### Web Resources

- 1. Parallelism-https://joehdesign.blogspot.com/2021/06/define-parallelism-in-computer.html.
- 2. Memory hierarchy-https://www.elprocus.com/memory-hierarchy-in-computer-architecture/

## CO Vs PO Mapping and CO Vs PSO Mapping

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	1	2	2	2	2	1					2	1			1
2	2	3	1	2	2		1		1		1	3		2	
3	2	2	1	2	1	2						2			2
4	3	3	2	2	1	1					1	1		3	
5	2	2	1	2	1	1					2	1			1

## $1 \rightarrow \text{Low } 2 \rightarrow \text{Medium } 3 \rightarrow \text{High}$

21VL2708	ELECTRONIC DESIGN AUTOMATION	L	Τ	Р	C
		3	0	0	3
Objectives					

- 1. To understand the special features of VLSI back end and front end CAD tools and Unix shell script
- 2. To study the synthesizable verilog and VHDL code.
- 3. To understand the Pspice code for any electronics circuit and to perform montecarlo analysis and sensitivity/worst case analysis.
- 4. To understand the difference between verilog and system verilog and are able to write system verilog code.
- To understand Cypress PSOC structure, modules and interconnects. 5.

UNIT I	AN OVER	VIEW OF OS COMMANDS		9
System settings	and configuration	Introduction to UNIX commands	. Writing	g Shell scripts. VLSI
design automati	ion tools. An overvi	ew of the features of practical CA	D tools.	Modelsim, Leonardo
spectrum, ISE 1	3.1i, Quartus II, VLS	I backend tools.		
UNIT II	SYNTHESIS A	AND SIMULATION USING HD	LS	9
Logic synthesi	s using verilog ar	nd VHDL. Memory and FSM	synthesis	. Performance driven
synthesis, Simu	lation- Types of sin	nulation. Static timing analysis. Fo	ormal ver	rification.Switch level
and transistor	level simulation.			
UNIT III	CIRCUIT	SIMULATION USING SPICE		9
Circuit descript	ion.AC, DC and tra	ansient analysis. Advanced spice c	ommands	s and analysis. Models
for diodes, tran	sistors and opamp. I	Digital building blocks. A/D, D/A	and sam	ple and hold circuits.
Design and anal	ysis of mixed signal c	circuits.		0
		YSTEM VERILOG		<u> </u>
Introduction, D	esign hierarchy, Data	a types, Operators and language co	onstructs.	Functional coverage,
Assertions, Inter	maces and test bench	structures. Wilked signal circuit mod	uening an	a analysis, Concept of
	ΙΝΤΟΛΟΙΟΤΙ	ON TO CUDESS DDOCDAMM	ARIE	0
UNII V	S	YSTEM ON CHIP (PSOC)	ADLE	9
Structure of PS	SoC, PSoC Designer	r, PSoC Modules, Interconnects, 1	Memory	Management, Global
Resources, and I	Design Examples.		•	
		Total	Periods	45
Suggestive Asso	essment Methods			
Continuous As	sessment Test	Formative Assessment Test	End Ser	mester Exams
(30 Mar	ks)	(10 Marks)	(60 Ma	rks)
2 Formativ	ve Multiple Choice	2 Online Ouizzes	1. 1	Formative Multiple
Question	IS	3. Problem Solving		Choice Questions
		Activities		
Outcomes				
Upon completio	on of the course, the	students will be able to:		
CO708. 1	Understand the spec Unix shell script	tal features of VLSI back end and fr	ont end C	AD tools and
CO708. 2	Write synthesizable	verilog and VHDL code.		
CO708. 3	Write Pspice code analysis and sensitiv	for any electronics circuit and to vity/worst case analysis.	perform	monte-carlo
CO708. 4	Understand the diffe system verilog code.	rence between verilog and system ve	rilog and	are able to write
CO708. 5	Understand Cypress	PSOC structure, modules and interco	onnects.	
Text Books				
1. M.J.S.St	nith, "Application Sp	ecific Integrated Circuits", Pearson, 2 PSpice using OrCAD for circuits and	2008. d electro	onics" Pearson 2004

#### **Reference Books**

- 1. Z. Dr Mark, "Digital System Design with System Verilog ", Pearson, 2010.
- Robert Ashby, "Designer's Guide to the Cypress PSoC, Newnes (An imprint of Elsevier)", 2006
   O.H. Bailey, "The Beginner's Guide to PSoC", Express Timelines Industries Inc.

## Web Resources

- 1. https://nptel.ac.in/courses/106/105/106105083/
- 2. http://www.nptelvideos.in/2012/11/electronic-design-and-automation.html

## CO Vs PO Mapping and CO Vs PSO Mapping

СО	PO1	PO2	PO3	PO4	PO5	PO6	<b>PO7</b>	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	3	2	2	3	1							3			1
2	3	3	3	2	3							3		2	
3	3	3	3	2	1							3			2
4	3	3	3	3	1							3		1	
5	3	3	3	3	3							3			1

1→Low 2→Medium 3→High

PROFESSIONA	AL ELECTIVE V				
21VL2709	Modelling and Simulation of Solid-State Circuits	3	0	0	3
21VL2710	Internet of Things	3	0	0	3
21VL2711	Hardware/Software Co-design	3	0	0	3
21VL2712	3D IC Design and Modeling	3	0	0	3
21VL2709	MODELLING AND SIMULATION OF SOLID-STATE	L	T	P	(
	CIRCUITS	3	0	0	3
Prerequisites for	the course		1		
CMOS VLS	Design				
Objectives					
1. To study the	basics of various device modelling				
2. To study an	d model MOS Transistors and MOS Capacitors				
3. To study an	d model MOS structures				
4. To understa	nd the various CMOS design parameters				
5. To study the	device level characteristics of BJT transistors				
	INTRODUCTION TO DEVICE MODELLING			9	
Surface Potential	Accumulation Depletion and Inversion Electrostatic P	otenti	ala	nd	Char
Distribution in Sili	con Capacitances in an MOS Structure MOS under Non-e	anilih	rium	n and	Gate
Diodes. Charge in	Silicon Dioxide and at the Silicon–Oxide Interface. Effect o	f Inte	rface	e Tra	ips ai
Dxide Charge on	Device Characteristics, High-Field Effects, Impact Ioniza	tion	and	Ava	alancl
Breakdown, Band-	o-Band Tunnelling, Tunnelling into and through Silicon Diox	kide,	Injec	tion	of H
Carriers from Silico	on into Silicon Dioxide, High-Field Effects in Gated Diodes, Die	lectri	c Bre	eakdo	own
UNIT II	MOSFET DESIGN			9	
The MOS Capacito	r-The field effect in bulk semiconductors-The ideal two-termin	al MC	S st	ructu	re. T
ong-Channel MC	SFET-Compact surface potential MOSFET models. Desig	n-orie	entec	I M	OSFF
nodel. dc Models-	Channel length modulation. Effect of source and drain resistant	ces. S	hort	and	narro
hannel effects, S	tored charges, Transit time, Capacitive coefficients, Noise	mod	eling	usi	ng tl
mpedance field me	thod, The y-parameter model, Compact model for tunneling in N	MOS	struc	tures	
UNIT III	ADVANCED MOSFET STRUCTURES AND MODELS FOR			9	
	CIRCUIT SIMULATORS				
Deep submicron pl	anar MOS transistor structures, Silicon-on-insulator (SOI) CMC	OS tra	nsist	ors, S	Surfa
otential- vs. invers	ion charge-based models, Charge-based models - The ACM mo	del -7	The E	EKV	mode
The BSIM5 model	Surface potential models - The HiSIM model-MOS model 11 -	The S	P mo	odel	
UNIT IV	CMOS DESIGN		-	9	
Basic CMOS Circu	it Elements, CMOS Inverters, CMOS NAND and NOR Gates	Inve	erter	and	NAN
avouts Parasitio	Elements Source-Drain Resistance Parasitic Canacitance	,	hate	Reci	istano
$\frac{1}{2} \frac{1}{2} \frac{1}$	C Songitivity of CMOS Delay to Device Democratic D	us, C		ICS.	
nuarconnact P and	C, Sensitivity of CNIOS Delay to Device Parameters, Propaga	uon I	Jelay	y and	Dela
		C	• , • •		
Equation, Delay Se	nsitivity to Channel Width, Length, and Gate Oxide Thickness	, Sen	sitivi	ity of	f Dela
Quation, Delay Se Power-Supply	nsitivity to Channel Width, Length, and Gate Oxide Thickness Voltage and Threshold Voltage, Sensitivity of Delay to Par	, Sen asitic	sitivi Res	ity of istan	f Dela ce ai
Equation, Delay Se Do Power-Supply Capacitance, Delay	nsitivity to Channel Width, Length, and Gate Oxide Thickness Voltage and Threshold Voltage, Sensitivity of Delay to Par of Two-Way NAND and Body Effect, Performance Factors	, Sen asitic of A	sitivi Res dvar	ity of istan iced	f Dela ce ai CMC

	UNIT V TRANSISTOR DESIGN 9														
n-	-p–n T	ransist	ors, B	asic O	peratio	n of a	Bipol	lar Tra	nsistor	, Modif	fying th	e Simp	le Diode	e Theor	y for
D	Describing Bipolar Transistors, Ideal Current–Voltage Characteristics, Collector Current, Base Current,														
C	urrent	Gains,	Ideal	IC-VC	CE Cha	racteri	stics,	Charac	eteristic	es of a '	Typical	n-p-n	Transist	or, Effe	ct of
E	mitter a	and Ba	ise Ser	ies Res	sistanc	es, Eff	ect of	Base-	Collect	tor Volt	age on	Collecto	or Curre	ent, Coll	ector
C	urrent	Fall of	f at Hi	gh Cui	rrents,	Non-ic	leal Ba	ase Cu	rrent a	t Low (	Currents	, Bipola	r Devic	e Mode	ls for
	rcuit a	nd Tin	ne-Dep	endent	Analy	ses Ba	ISIC dc	Mode	I, Basic	ac Mo	del, Sm	all-Sign	al Equiv	valent C	ircuit
N	odel, E	mitter	Diffus	sion Ca	ipacitai	nce, Cr	harge-	contro	I Analy	/sis, Bre	akdowr	i Voltag	ges,	45	
Sı	iggest	ive As	sessm	nent M	ethod	s					nai r ei	lous		45	
C	ontinu	ous A	ssessi	nent 7	ſest	Fo	rmati	ve Ass	sessme	ent Tes	t E	nd Sem	lester E	Exams	
	(3	0 Mar	·ks)				(1	l 0 Mai	rks)		(6	60 Mar	ks)		
	1. D	) escrip	tion Q	uestio	ns		1. As	ssignm	nent			1. D	escripti	on	
	<b>2.</b> F	'ormat	ive Mi	iltiple	Choice	9	2. 0	nline (	)uizzes	5		Q	uestion	s	
	Q	uestic	ns				<b>3.</b> Pr	oblem	n Solvii	ng		<b>2.</b> Fo	ormativ	e Multij	ple
							A	ctivitie	es			Cl	hoice Q	uestion	5
0	utcom	es													
U	pon co	omple	tion of	f the c	ourse	, the s	tuden	ts wil	l be ab	ole to:					
	CO7	09.1	To de	esign a	nd moo	del MC	DSFET	and B	JT dev	rices to o	desired s	specifica	ations		
	CO7	09.2	To u	ndersta	ind the	physic	s behi	nd the	device	operati	on				
	CO7	09.3	To an	nalyse	the imp	bact of	the de	vice pl	nysics i	in circui	it design	l			
CO709. 4 To model novel semiconductor devices															
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	<b>4.</b> .J	P COI	inige, v		oninge,	Phys		Semico	onduct	or devic	es spr	inger 20		IOII.	
R	eferen	ice Bo	oks												
	1. Y	uan Ta	aur and	l Tak F	I. Ning	. "Fun	damen	tals of	Mode	rn VLSI	Device	s". Carr	bridge l	Universi	tv
	P	ress, S	econd	Edition	n, 2009	,, 1 un	Guinen	<i>iuis</i> 01	111040		20,100	, cui			, y
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#### 21VL2710

### INTERNET OF THINGS

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#### **Prerequisites for the course**

• The pre-requisite knowledge required by the Students to study this Course is basic knowledge in Embedded Systems.

#### **Objectives**

- 1. To understand characteristics and design of IoT.
- 2. To gain knowledge in IoT design Methodology.
- 3. To develop various applications in IoT using Python Programming.
- 4. To analyse the advancements of Internet in mobile Device, Cloud & amp; Sensor Networks.
- 5. To understand the need for security in IoT enabled systems.

### UNIT I INTRODUCTION TO INTERNET OF THINGS

Introduction – Physical Design of IoT – Logical Design of IoT – IoT Enabling Technologies – IoT Levels and Deployment Templates – Domain Specific IoTs: Home Automation, Cities, Environment, Energy, Retail, Logistics, Agriculture, Inductry, Healthcare and Lifestyle – IoT Design Methodology.

#### UNIT II

#### IOT, M2M & IOT SYSTEM MANAGEMENT

Introduction – M2M, Difference between IoT and M2M – Software Defined Networking, Network Function Visualization – Need for IoT System Management – Simple Network Management Protocol – Network Operator Requirements – NETCONF – YANG, IoT System Management with NETCONF – YANG - NETOPEER.

UNIT III	IOT LOGICAL DESIGN USING PYTHON	9
Introduction – Py	thon Datatypes and Structure – Control Flow – Functions – Mod	ules – Packages – File
II. II. D. (	Time Orantican Classes Dether Dethers for LT. ICC	NI VIAL LITTEL !!.

Handling – Date/Time Operations – Classes – Python Packages for IoT: JSON, XML, HTTPLib, URLLib, SMTPLib.

UNIT IV	IOT PHYSICAL DEVICES, SERVERS AND CLOUD	9
	OFFERINGS	

Basic Building Block of IoT, Exemplary Device: Raspberry Pi, Interfaces, Programming Raspberry Pi with PYTHON, Other IoT Devices: BeagleBone Black, Intel Galileo, Microcontroller, System on Chips - IoT system building blocks - Arduino, IDE programming - Introduction to Cloud Storage models & Communication APIs - Amazon Web Services for IoT.

## UNIT V

Need for encryption, standard encryption protocol, light weight cryptography, Quadruple Trust Model for IoT-A – Threat Analysis and model for IoT-A, Cloud security.

IoT SECURITY

	Periods	45			
<b>Suggestive Assessment Methods</b>					
Continuous Assessment Test	Formative Assessment Test	End Semester Exams			
(30 Marks)	(10 Marks)	(60 Ma	rks)		
1. Description Questions	1. Assignment	1. I	Description		
<b>2.</b> Formative Multiple Choice	2. Online Quizzes	(	Questions		
Questions	3. Problem Solving	<b>2.</b> I	Formative Multiple		
	Activities	(	Choice Questions		

Outco	mes
Upon	completion of the course, the students will be able to:
CC	0710. 1 Understand the various design aspects of Internet of things
CC	O710. 2 Critically evaluate ethical and potential security issues related to the Internet of
	Things
CC	0710. 3 Design IoT system using Python Programming
CC	1710. 4 Implement new applications based on Raspberry Pi ,Intel Galileo and Arduino board
CC	0710. 5 Analyse the need for security in Internet of Things
Text <b>B</b>	Books
1.	Arshdeep Bahga, Vijay MadisettiInternet of Things - A hands-on approach, Universities
	Press, 2015.
2.	Olivier Hersent, David Boswarthick, Omar Elloumi - The Internet of Things: Key Applications
	and Protocols, Wiley, 2012
Refer	ence Books
3.	Adrian McEwen, Hakim Cassimally - Designing the Internet of Things, Wiley, 2013
4.	Peter Waher - Mastering Internet of Things: Design and create your own IoT applications using
	Raspberry Pi 3, Packt, 2018.
5.	Gaston C. Hillar - Internet of Things with Python, Packt, 2016.
6.	RonaldL. Krutz, Russell Dean Vines, Cloud Security: A Comprehensive Guide to Secure Cloud
	Computing, Wiley-India, 2010
Web F	Resources
1.	https://onlinecourses.nptel.ac.in/noc21_cs17/preview_
2.	https://www.coursera.org/specializations/iot
3.	https://www.edx.org/course/introduction-to-the-internet-of-things-iot

СО	PO1	PO2	PO3	PO4	PO5	PO6	<b>PO7</b>	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	3	3	3		3					2	2			2	
2	3	3	3		3					2	2	2			
3	3	3	3		3					2	2		2		
4	3	3	3		3					2	2				
5	3	3	3		3					2	2		1		

# $1 \rightarrow \text{Low } 2 \rightarrow \text{Medium } 3 \rightarrow \text{High}$

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Prerequisites for	r the course		I						
System Des	System Design, Embedded Design and Development Systems								
Ubjectives	-1-illa for taking 1	the frame and hardware day	in math	ada tu	- coli		lay		
1. To develop	SKIIIS IOF TAKING U	best from software and naroware des	ign metn	oas u	) SOIV	ve com	npiex		
2 To familiar	esign problem.	een flevihility and performance							
2. To further $3$ To effective	vely use the secu	uential way of decomposition in t	ime and	the -	narall	lol wa	w of		
decomposit	ion with space usi	no hardware		the	paran	CI wa	ly Or		
4 To understa	and the data flow n	nodeling and analysis							
5. To study at	bout system on chir	p and on-chip busses							
		CO-DESIGN CONCEPTS				9			
Introducing Hardy	vare/Software Cod	lesign- The Ouest for Energy Effici	iencv- Tł	ne Dr	iving	Facto	ors in		
Hardware/Software	e Codesign- The	Hardware–Software Codesign Spac	e- The I	Dualis	m of	f Hard	lware		
Design and Softwa	re Design- Abstra	ction Levels- Concurrency and Paralle	elism- Pro	oblem	ns -				
2	10	//////////////////////////////////////	<b>U</b> 1101	0011					
UNIT II	DATA FLO	W MODELING AND ANALYSIS				9			
The Need for Cor	current Models: A	An Example- Analyzing Synchronou	ıs Data F	Flow	Grapl	hs- Co	ontrol		
Flow Modeling ar	nd the Limitations	of Data Flow Models- Software I	mplemen	tation	ı of I	Data F	Flow-		
Hardware Impleme	entation of Data F	Flow- Data and Control Edges of a	C Progra	ım- D	)ata a	und Co	ontrol		
Edges of a C Prog	gram- Construction	n of the Control Flow Graph - Con	struction	of th	ne Co	ontrol	Flow		
Graph									
	CUCTEM	AND AND AND ON CHID BUCCE	9						
UNIT III	SISIEIVI	ON CHIP AND UN-UNIF DUDDE	S Condia Sy	-tom	50	9 <u>- Mad</u>	Lag		
The System-on-on-on-on-on-on-on-on-on-on-on-on-on-	ip Concept- SUC P	Architecture- Example: Fortable Mun		ystem	1- DUN N 1-11-1		leiing		
In GEZEL- Connec	Sting Hardware and	d Software, On-Chip bus systems- D	Sus Trans	ters-	Mum	masic	r Bus		
Systems- On-Cmp		ADE SOFTWADE INTEDEACES	•			<u></u>			
UNIT IV	nanu u	AKE/SUF I WARE INTERFACED	Mamor	y vrv Manned Interfaces					
Introduction to ma	If a Ware/Soliware	Interface- Synchronization Schemes	- Menior	y-iviaj	ppeu	IIICII	aces-		
		OP CONTROL SHELL DESIGN	4 NID			0			
UNIIV	UUINULID	APPLICATIONS				9			
The Coprocessor C	Control Shell- Data	Design- Control Design- Programm	er's Mod	el = C	Contro	ol Des	ign +		
Data Design- AES	S Encryption Cop	rocessor- Trivium Stream Cipher A	lgorithm-	Coo	rdina	te Rot	tation		
Digital Computer	Algorithm- Harc	lware Coprocessor for CORDIC-	Handling	Lar	ge A	moun	ts of		
Rotations		L L			5				
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		Total P	eriods	45					
Suggestive Asses	sment Methods								
Continuous Asse	ssment Test	Formative Assessment Test	End Ser	neste	er Ex	ams			
(30 Marks)	)	(10 Marks)	(60 Mai	arks)					
1. Description	n Questions	1. Assignment	1. E	)escri	iptio	n			
<b>2.</b> Formative	Multiple Choice	2. Online Quizzes	Questions						
Questions		<b>3.</b> Problem Solving	<b>2.</b> Formative Multipl			ple			

Francis Xavier Engineering College | Department of ECE |M.E-VLSI | R2019 | Curriculum and Syllabi 2021 72 Activities **Choice Questions Outcomes** Upon completion of the course, the students will be able to: CO711.1 To acquire the knowledge about hardware/software codesign. CO711.2 To learn the formulation of partitioning the hardware and software. CO711.3 To learn the concept of system on chip and on chip buses. CO711.4 To study the hardware/software interfaces. CO711.5 To design hardware/software interfaces for different applications. **Text Books** 1. Patrick Schaumont "A Practical Introduction to Hardware/Software Co-design", Patrick Schaumont, Springer, 2012. **Reference Books** 1. Ralf Niemann, "Hardware/Software Co-Design for Data Flow Dominated Embedded Systems", Kluwer, 1998. 2. Alxel Jantsch, "Modeling Embedded Systems and SOC's. Concurrency and Time in Models of Computation", MK, 2004. Web Resources https://link.springer.com/book/10.1007/978-1-4614-3737-6#about CO Vs PO Mapping and CO Vs PSO Mapping PO2 PO3 PO4 PO5 **PO6 PO7 PO8 PO9 PO10** PO11 **PO12** PSO1 PSO2 PSO3 CO **PO1** 2 1 3 3 2 3 2 1 3 2 3 3 3 3 3 1 3 3 3 3 1 1 2 4 3 3 3 3 3 1 3 5 3 3 3 3 3 1 3 1  $1 \rightarrow Low 2 \rightarrow Medium 3 \rightarrow High$ 21VL2712 **3D IC DESIGN AND MODELING** L Т Ρ С 3 0 0 3 Prerequisites for the course The pre-requisite knowledge required by the Students to study this Course is basic knowledge in • VLSI Design. **Objectives** 1. Understand the basics of 3D IC design. 2. Model the through silicon Vias.
- 3. To get an overview on electrical performance and signal integrity.
- 4. Review and discuss the power distribution in 3D ICs
- 5. To discuss the alternate methods for power distribution

UNIT I	SYSTEM INTEGRATION AND MODELING					
	CONCEPTS					

Moore's Law, IC Integration Vs System Integration, History of Integration, Primary Drivers for 3D Integration, Role of the Interposer in 3D Integration, Modeling and Simulation

9

UNIT II	ELECTRICAL MODELING OF THROUGH SILICON	9
	VIAS	

Benefits of Through Silicon Vias, Challenges in Modeling Through Silicon Vias, Propagating Modes in Through Silicon Vias, Physics Based Modeling of Through Silicon Vias, Modeling of Conical Through Silicon Via, MOS Capacitance Effect

UNIT III	ELECTRICAL PERFORMANCE AND SIGNAL	9
	INTEGRITY	

Process Optimization, Cross Talk in Interposers, Via Arrays, Interposers, Modeling and Design Challenges

UNIT IV	POWER	DISTRIBUTION,	RETURN	PATH	9	
	DISCONTINUITIES AND THERMAL MANAGEMENT					

Power Distribution, Power Distribution for 3D Integration, Current Paths in IC and Package, Signal and Power Integrity, Challenges for Addressing Power Distribution in 3D ICs and Interposers, Thermal Management and its Effect on Power Distribution, .

UNIT V	ALTERNATE METHODS FOR POWER	9
	DISTRIBUTION	

Introducing Power Transmission Lines, Constant Current Power Transmission Line, Pseudo Balanced Power Transmission Line, Constant Voltage Power Transmission Line, Power Calculations, Application of Power Transmission Lines to FPGA, Managing Signal and Power Integrity for 3D ICs.

	Total	Periods	45
Suggestive Assessment Methods			
<b>Continuous Assessment Test</b>	Formative Assessment Test	End Se	mester Exams
(30 Marks)	(10 Marks)	(60 Ma	rks)
1. Description Questions	1. Assignment	1. 1	Description
<b>2.</b> Formative Multiple Choice	2. Online Quizzes	(	Questions
Questions	3. Problem Solving	2.	Formative Multiple
	Activities		Choice Questions
Outcomes			
Upon completion of the course, t	he students will be able to:		
CO712. 1 Model through silico	on vias.		
CO712. 2 Analyse the electrica	al performance.		
CO712. 3 Design the power di	stribution architecture.		
CO712. 4 Perform the thermal	management.		
CO712. 5 Overcome the design	n challenges.		
Text Books			

- 1. Madhavan Swaminathan, Ki Jin Han, "DESIGN AND MODELING FOR 3D ICs AND INTERPOSERS" World Scientific Publishing, 2014.
- 2. Paul D. Franzon, Erik JanMarinissen, andMuhannad S. Bakir, "Handbook of 3D Integration", Wiley, 2019

## **Reference Books**

- 1. Lajos Hanzo, "Electrical Modeling and Design for 3D System Integration", Wiley, IEEE Press, 2012
- 2. Anantha Chandrakasan, "Integrated Circuits and Systems", Springer, 2010

## Web Resources

- 1. https://www.gsaglobal.org/wp-content/uploads/2012/06/3D-IC-Architecture.pdf
- 2. https://www.cadence.com/content/dam/cadence-www/global/en\_US/documents/solutions/3d-ic-design-wp.pdf
- 3. https://blogs.synopsys.com/from-silicon-to-software/2021/03/04/3dic-design-tools
- 4. https://www.cadence.com/en\_US/home/solutions/3dic-design-solutions.html

# CO Vs PO Mapping and CO Vs PSO Mapping

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	3		2												3
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5	3		2	2	2										2

# 1→Low 2→Medium 3→High

PROFESSIONAL ELECTIVE VI									
21VL2713	Embedded System and RTOS	3	0	0	3				
21VL2714	VLSI for Biomedical Applications	3	0	0	3				
21VL2715	Advanced Microprocessors and Architectures	3	0	0	3				

21VL2713	21VL2713 EMBEDDED SYSTEMS AND RTOS			Р	С
		3	0	0	3

#### Prerequisites for the course

• The pre-requisite knowledge required by the Students to study this Course is basic knowledge in Computer Architecture.

## Objectives

- 1. To introduce the basics of embedded systems and ARM Processor.
- 2. To understand the basics of CPU and the bus operations.
- 3. To hone the process inside the processor and networking operations in embedded environment.
- 4. To master the basics of Realtime operating systems.
- 5. To design an Real time operating systems.

### UNIT I EMBEDDED COMPUTING & ARM PROCESSOR

9

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Embedding Computers - Characteristics of Embedded Computing Applications - Challenges in Embedded Computing System - The Embedded System Design Process - Formalisms for System Design -Computer Architecture Taxonomy - Assembly Language - ARM Processor: Memory Organization -Data Operations - Flow of Control.

	UNIT II			CPUs	s AND	BUS	50	PER	ATION	S
-		-	1.0	ä		3.5		-	•	1 -

Programming Input and Output - Supervisor Mode, Exceptions, and Traps - Co-Processors -Memory System Mechanisms - CPU Performance - CPU Power Consumption - CPU Bus - Memory Devices - I/O devices - Component Interfacing - Designing with Microprocessors - Development and Debugging - System-Level Performance Analysis.

PROCESSES AND NETWORKS

9

Multiple Tasks and Multiple Processes - Preemptive Real-Time Operating Systems - Priority-Based Scheduling: Rate-Monotonic Scheduling, Earliest-Deadline-First Scheduling - Power Management and Optimization for Processes - Networks for Embedded Systems - Internet-Enabled Systems - Vehicles as Networks - Sensor Networks.

UNIT IV	<b>REAL TIME OPERATING SYSTEM</b>	9					
Survey of Software Architectures: Round robin Architecture, Round robin with interrupt, Function queue							
scheduling architecture Realtime Operating system Architecture – Task and Task States – Semaphores							
and Shared Data - Message Queues, Mailboxes and Pipes - Timer Functions - Events - Memory							
Management – Interrupt Routine in RTOS environment.							

	UNI	IT V		DESIGNING USING RTOS 9													
En	Encapsulating Semaphores and Queues - Hard realtime scheduling considerations - Saving memory																
spa	space - saving power - Software Development tools - Host machine and target machine - Linker																
Lo	Locator for Embedded Software – getting embedded softwares in to target systems – Testing your host																
ma	achine	– instr	uction	set sin	nulators	•											
										То	tal Per	riods		45			
Su	ggest	ive As	sessm	ient M	lethod	5											
Co	ntinu	ous A	ssessr	nent 7	ſest	For	rmativ	ve Ass	essme	ent Tes	t E	nd Sem	ester E	Exams			
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01	itcom	AC							:5		I			1030000	,		
Ur	Unon completion of the course, the students will be able to:																
10	CO713. 1 Analyse the functions of the components in Embedded Systems																
	CO713. 2 Design the hardware and software components in embedded field																
	CO713.2 Design the hardware and software components in embedded field CO713.3 Design scheduling algorithms in multiprocessors and operating systems																
	CO713. 4 Understand the concept of Real Time Operating Systems																
	CO713.5 Design a Real Time Operating systems																
Τe	ext Bo	oks		<u></u>		<u> </u>	0										
	1. V	Vavne	Wolf, '	"Comr	miters as	Com	nonent	ts - Pri	ncinles	ofEmb	edded (	Compute	er Svste	m Desig	'n''.		
	2	nd Edi	tion, N	lorgan	Kaufm	ann Pi	ublishe	er, 200	8.	01 2	euue		01 0 9 2 1 2	III D	<b>II</b> ,		
	2. D	David E	E Simo	n, "An	Embed	ded So	oftwar	e Prim	er", 2 <sup>nd</sup>	<sup>d</sup> Editior	n, Pearso	on Educ	ation, 1	999			
Re	eferen	ice Bo	oks														
	1. X	Ciaocor	ng Fan	. "Rea	l Time	Embe	dded S	System	n – Des	sign Pri	nciples	and Eng	gineerin	g Practi	ces",		
	N	Jewnes	s Elsev	vier, 20	)15.			-		-	-						
	2. Ji	iacun v	vang, "	Real T	`ime En	nbedd	ed Sys	tems",	John V	Wiley &	Sons, I	nc, 201'	7.				
	3. K	C.C. W	ang. "	Embed	ded and	d Real	l Time	Opera	ating S	ystems	', Spring	ger Inter	rnationa	l Publis	hing,		
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	4. C	Colin V	Valls, `	'Buildi	ing a R	eal Tr	ime O	peratin	ig Syst	em RTC	OS from	n the G	round U	Jp", Els	evier		
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CO	PO1	PO2	PO3	PO4	PO5	PO6	<b>PO7</b>	PO8	<b>PO9</b>	PO10	PO11	PO12	PSO1	PSO2	PSO3		
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l	5	-	-	<u> </u>						-	2						

# $1 \rightarrow Low 2 \rightarrow Medium 3 \rightarrow High$

21VL2714	VLSI FOR BIOMEDICAL APPLICATIONS	L	Т	Р	С				
		3	0	0	3				
Prerequisites fo	r the course								
Analog and	d Digital IC Design								
Objectives									
1. To study the	he biomedical amplifiers, filters and analog to digital converters.								
2. To underst	and the structure and operation of implantable medical devices.								
3. To get an o	overview on non invasive medical electronics.								
4. To review	the ultra-low-power analog and digital design principles.								
5. To discuss	the energy-harvesting circuits and energy sources								
UNIT I	LOW-POWER ANALOG BIOMEDICAL CIRCUITS			9					
Low power trans i	mpedance amplifiers and photoreceptors, Low power trans cond	uctanc	e am	plifier	s and				
scaling laws for p	ower in analog circuits, Low-power filters and resonators, Low	power	r curi	rent -	mode				
circuits, Ultra-low	-power and neuron-inspired analog-to-digital conversion for bior	nedica	ıl sys	tem					
	III TRA-I OW-POWER IMPLANTABLE MEDICAL			9					
	ELECTRONICS			,					
Introduction, Coc	hlear implants or bionic ears, An ultra-low-power programma	ble ar	nalog	bioni	c ear				
processor, Low-power electrode stimulation, Highly miniature electrode-stimulation circuits, Brain-									
machine interfaces	s for the blind, Brain-machine interfaces for paralysis, speech, an	d othe	r disc	orders.					
UNIT III	ULTRA-LOW-POWER NONINVASIVE MEDICAL			9					
Introduction Anal	ag integrated-circuit switched-capacitor model of the heart the	e elect	roca	rdiogra	am a				
micropower electr	ocardiogram amplifier. Low-power pulse oximetry. Battery-free	e tags	for t	odv s	ensor				
networks, Intra-bo	dy galvanic communication networks, Biomolecular sensing	0		j					
		ſ							
UNIT IV	PRINCIPLES FOR ULTRA-LOW-POWER ANALOG			9					
	AND DIGITAL DESIGN								
Sizing and topolo	gies for robust sub threshold operation digital design, Types	of po	wer	dissipa	ation,				
Energy efficiency	and optimization in digital systems, Varying the power-supply	voltag	ge an	d thre	shold				
voltage, Gated clo	cks, Basics of adiabatic computing, Architectures and algorithms	for in	nprov	ving ei	nergy				
efficiency, Power	consumption in analog and digital systems, The optimum point	nt for	digiti	ization	in a				
mixed-signal syste	em, The Shannon limit for energy efficiency, Collective analog of	or hyb	rid co	omputa	ation,				
HSMs: general-pu	rpose mixed-signal systems with feedback - General principles	for lo	w-po	wer m	ixed-				
signal system desi	gn, Sensors and actuators.								
UNIT V	ENERGY-HARVESTING CIRCUITS AND ENERGY	9							
	SOURCES								
Wireless inductive	e power links for medical implants, Energy-harvesting RF anter	na po	wer	links,	Low-				
power RF telemet	ry in biomedical implants, Batteries and electrochemistry, Ener	gy ha	rvesti	ing an	d the				
future of energy									

Francis Xavier Engineering College | Department of ECE |M.E-VLSI | R2019 | Curriculum and Syllabi 2021 78 **Total Periods** 45 Suggestive Assessment Methods **Continuous Assessment Test Formative Assessment Test End Semester Exams** (30 Marks) (10 Marks) (60 Marks) 1. Description Questions 1. Assignment 1. Description **2.** Formative Multiple Choice 2. Online Quizzes Questions Questions **3.** Problem Solving **2.** Formative Multiple Activities **Choice Questions Outcomes** Upon completion of the course, the students will be able to: Design biomedical amplifiers, filters and analog to digital converters.. CO714.1 CO714.2 Explain the concept of implantable medical devices Understand the noninvasive medical electronics. CO714.3 CO714. 4 Analyse the ultra-low-power analog and digital design principles. CO714.5 Contribute to the development energy-harvesting circuits for biomedical devices. **Text Books** 1. Rahul Sarpeshkar, 'Ultra Low Power Bioelectronics: Fundamentals, Biomedical Applications, and Bio-inspired Systems', Cambridge University Press, 2010 **Reference Books** 1. R.S. Khandpur, 'Handbook of Biomedical Instruments'Third Edition, McGraw Hill, 2014 2. Krzysztof Iniewski, 'CMOS Biomicrosystems where Electronics Meet Biology', Wiley, 2011 Web Resources Technology, https://www.sciencedirect.com/topics/computer-science/memory-1. Memory technology 2. Reliability Point of Semiconductor Memories from Practical of View. a https://link.springer.com/chapter/10.1007%2F978-3-322-83629-8 22 memory-Materials 3. Advanced for of information technology, a new era https://doi.org/10.1557/mrs.2018.96 CO Vs PO Mapping and CO Vs PSO Mapping **PO1** PO2 PO3 **PO4 PO7** PO12 PSO1 PSO3 CO PO5 **PO6 PO8 PO9 PO10 PO11** PSO2 2 1 3 2 2 2 2 2 3 3 3 1 2 4 2 3 5 1 1 1  $1 \rightarrow Low 2 \rightarrow Medium 3 \rightarrow High$ 

rancis Xavier Engineeri	ng College   Depa	rtment of ECE /M.E-VLSI / R2019 / Cui	riculum d	and Sy	llabi	2021	79				
21VL2715	ADVAN	CED MICROPROCESSORS ANI ARCHITECTURES	L	T	Р	C					
				3	0	0	3				
Prerequisites for	the course										
• Analog and I	Digital IC										
Objectives											
1. Study the Ar	chitecture of 808	6 microprocessor.									
2. Learn the de	2. Learn the design aspects of I/O and Memory Interfacing circuits.										
3. Study about	communication a	nd bus interfacing.									
4. Study the Ar	chitecture of 805	1 microcontroller.									
5. Understand t	he advanced arch	itectures									
UNIT I	8086 MICI	<b>ROPROCESSOR ARCHITECTUI</b>	RE			9					
Introduction to 808 language programm Macros – Interrupts	6 – Microproces ing – Modular and interrupt serv	sor architecture – Addressing mod Programming - Linking and Reloc vice routines	es - Instr ation - S	uction stacks	i set– - Pr	- Asse cocedu	embly res –				
UNIT II	ADV	ANCE ARCHITECTURES		9							
8086 signals – Basi	c configurations	- System bus timing -Introduction	to Multipi	rograr	nmin	g – S	ystem				
Bus Structure – Mi configurations – Intr	ultiprocessor con oduction to Adva	figurations – Coprocessor, Closely anced processors	coupled	and	loose	ly Co	upled				
UNIT III	INTER	FACING AND CASE STUDIES				9					
Memory Interfacing	and I/O interfaci	ng - Parallel communication interfac	e – Serial	comr	nunic	cation					
interface – D/A and controller – Program display.	A/D Interface - <sup>7</sup> mming and appl	Timer – Keyboard /display controlle ications Case studies: Traffic Ligh	er – Interr t control,	upt co LED	ontrol disp	ller – olay ,	DMA LCD				
UNIT IV		MICROCONTROLLER				9					
Architecture of 80 Addressing modes -	51 – 8051 Pin Assembly langua	diagram, Special Function Registage programming.	ters (SFR	Rs) -	Instr	ruction	ı set-				
UNIT V	INTERI	FACING MICROCONTROLLER				9					
Programming 8051 ' Memory Interface- Controller.	Timers – LCD & Stepper Motor a	Keyboard Interfacing - ADC, DAC and Waveform generation, Keyboar	& Sensor d display	Inter inter	facing face	g - Ex and A	terna Alarm				
	Periods	45									
Suggestive Assess	ment Methods										
Continuous Asses (30 Marks)	sment Test	Formative Assessment Test (10 Marks)	End Ser (60 Ma	emester Exams arks)							
1. Description	Questions	1. Assignment	1. Assignment1. D				Description				
<b>2.</b> Formative M	Iultiple Choice	2. Online Quizzes	(	Quest	ions						
Questions		<b>3.</b> Problem Solving	<b>2.</b> I	Forma	ative	Multi	ple				
		Activities Choice Ques					S				

## Outcomes

### Upon completion of the course, the students will be able to:

CO716. 1 Design and implement programs on 8086 microprocessor.

CO716. 2 Design I/O circuits.

CO716. 3 Design Memory Interfacing circuits.

CO716. 4 Design and implement 8051 microcontroller based systems.

CO716. 5 Interface microcontroller with keyboard, ADC, DAC and sensors

### **Text Books**

 Yu-Cheng Liu, Glenn A.Gibson, "Microcomputer Systems: The 8086 / 8088 Family -Architecture, Programming and Design", Second Edition, Prentice Hall of India, 2007.
Mohamed Ali Mazidi, Janice GillispieMazidi, RolinMcKinlay, "The 8051 Microcontroller and Embedded Systems: Using Assembly and C", Second Edition, Pearson Education, 2011

### **Reference Books**

1. Doughlas V.Hall, "Microprocessors and Interfacing, Programming and Hardware:, TMH, 2012

### Web Resources

- 1. <u>https://www.electronicdesign.com/technologies/microprocessors/article/2179972</u> 9/advanced-microprocessor-bus-architecture-amba-bus-system
- 2. <u>https://www.mheducation.co.in/advanced-microprocessor-and-peripherals-9781259006135-india</u>
- 3. <u>http://people.bu.edu/bkia/sc757.htm</u>

## CO Vs PO Mapping and CO Vs PSO Mapping

СО	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	2		2											2	
2	3	3													1
3	1	2											2		
4	2		1												
5	2	1												3	

 $1 \rightarrow Low 2 \rightarrow Medium 3 \rightarrow High$