FRANCIS XAVIER ENGINEERING COLLEGE
AUTONOMOUS INSTITUTION
ACCREDITED BY NBA
ISO 9001:2015 Certified | DST-FIST Supported Institution
Recognized under Section 2(f) & 12(B) of the UGC Act, 1956
Vannarpettai, Tirunelveli - 627003, Tamil Nadu

# CURRICULUM & SYLLABUS

## M.E – VLSI Design

## Regulations 2019

## VISION OF THE DEPARTMENT

To develop Electronics and Communication Engineers by permeating with proficient morals, to be recognized as an adroit engineer worldwide and to strive endlessly for excellence to meet the confronts of our modern society by equipping them with changing technologies, professionalism, creativity research, employability, analytical, practical skills and to excel as a successful entrepreneur.

## MISSION OF THE DEPARTMENT

- To provide excellence through effective and qualitative teaching-learning process that equips the students with adequate knowledge and to transform the students' lives by nurturing the human values to serve as a precious resource for Electronics and Communication Engineering and nation.
- To enhance the problem solving and lifelong learning skills that will enable by edifying the students to pursue higher studies and career in research.
- To create students with effective communication skills, the abilities to lead ethical values in order to fulfill the social needs

**FRANCIS XAVIER ENGINEERING COLLEGE, TIRUNELVELI**

**DEPARTMENT OF ELECTRONICIS AND COMMUNICATION ENGINEERING**

**103 G2 Bye Pass Road, Vannarpettai, Tirunelveli, Tamilnadu – 627003**

**Phone : 0462 – 2502283, 2502157, Fax: 0462 – 2501007**

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## PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

**PEO 1 – Meet Market Demands :** Graduates will become a successful engineer to meet the demand driven needs of industries/technical profession

**PEO 2 – Core Competence:** Graduates will demonstrate core competence in mathematical, scientific and basic engineering fundamentals necessary to formulate, analyze and solve engineering problems and/or also to pursue advanced study or research

**PEO 3 – Design and Analysis:** Graduates will demonstrate good breadth of knowledge in core areas of Information Technology and related engineering so as to comprehend engineering trade-offs, analyze, design, and synthesize data and technical concepts to create novel designs in solving the real life problems

**PEO 4 – Professional Responsibility:** Graduates will demonstrate professional responsibility by offering a wide spectrum of consultancy and testing services by addressing social, cultural, economic, sustainability, and environmental considerations in the solution of real world engineering problems

**PEO5 – Life-long Learning:** Graduates will engage themselves in life-long learning through independent study and by participating in professional activities or continuing education

## PROGRAM OUTCOMES (POs)

**Engineering Graduates will be able to:**

**a. Engineering Knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

**b. Problem Analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

**c. Design/Development of Solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

**d. Conduct Investigations of Complex Problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

**e. Modern Tool Usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

**f. The Engineer and Society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

**g. Environment and Sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

**h. Ethics**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

**i. Individual and Team Work**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

**j. Communication**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

**k. Project Management and Finance**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

**l. Life-Long Learning**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

## PROGRAMME SPECIFIC OUTCOMES (PSOs)

1. **$PSO_a$ –** An ability to analyze a problem, design algorithm, identify and define the computing requirements appropriate to its solution and implement the same in emerging technology environments like cloud computing, embedded products and real-time systems..
2. **$PSO_b$ –** Knowledge of data and its management techniques for data acquisition, big data, handling of data etc. and enabling students in solving problems using these techniques of data analytics like pattern recognition, knowledge discovery.

## MAPPING OF PROGRAMME EDUCATIONAL OBJECTIVES WITH PROGRAMME OUTCOMES

A broad relation between the programme objective and the outcomes is given in the following table

| PROGRAMME EDUCATIONAL OBJECTIVES(PEO) | PROGRAMME OUTCOMES (PO) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **A** | **b** | **c** | **D** | **e** | **f** | **g** | **h** | **i** | **J** | **k** | **l** |
| **PEO 1** | | | | H | | | | L | L | M | M | L |
| **PEO 2** | H | H | L | L | | | | | | | | M |
| **PEO 3** | | | H | | | L | | | | | | H |
| **PEO 4** | | | H | | L | M | H | L | | | | |
| **PEO 5** | | | | | | | | | | | | H |

## MAPPING OF PROGRAMME SPECIFIC OBJECTIVES WITH PROGRAMME OUTCOMES

A broad relation between the Program Specific Objectives and the outcomes is given in the following Table

| PROGRAMME SPECIFIC OBJECTIVES(PEO) | PROGRAMME OUTCOMES (PO) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **A** | **b** | **c** | **D** | **e** | **f** | **g** | **h** | **i** | **J** | **k** | **l** |
| **$PSO_a$** | H | M | | | H | | | | M | M | | |
| **$PSO_b$** | | | | H | | | H | H | | | H | |

Contribution L: Low / Reasonable M: Medium / Significant H:High / Strong

**M.E VLSI DESIGN**

**REGULATIONS 2019**

**CHOICE BASED CREDIT SYSTEM**

| S. No | CATEGORY | CREDITS PER SEMESTER | | | | TOTAL CREDIT | CREDITS IN % |
|---|---|---|---|---|---|---|---|
| | | I | II | III | IV | | |
| 2 | ES | **4** | | | | **4** | **6%** |
| 3 | PC | **14** | **12** | | | **26** | **37%** |
| 4 | PE | **3** | **9** | **9** | | **21** | **30%** |
| 5 | EEC | | **1** | **6** | **12** | **19** | **27%** |
| **TOTAL** | | **21** | **22** | **15** | **12** | **70** | **100%** |

**SUMMARY OF CREDIT DISTRIBUTION**

ES - Engineering Sciences

PC - Professional Core

PE - Professional Elective

EEC - Employability Enhancement Course

**M.E VLSI DESIGN**

**REGULATIONS 2019**

**CHOICE BASED CREDIT SYSTEM**

**I – IV SEMESTERS CURRICULA AND SYLLABI**

| **FIRST SEMESTER** | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Code No.** | **Course** | **Category** | **L** | **T** | **P** | **C** | **H** |
| 19MA1255 | Advanced Applied Mathematics | ES | 3 | 1 | 0 | 4 | 4 |
| 19VL1601 | Advanced Digital System Design | PC | 3 | 0 | 0 | 3 | 3 |
| 19VL1602 | Analog IC Design | PC | 3 | 0 | 0 | 3 | 3 |
| 19VL1603 | CAD for VLSI circuits | PC | 3 | 0 | 0 | 3 | 3 |
| 19VL1604 | Digital CMOS VLSI Design | PC | 3 | 0 | 0 | 3 | 3 |
| | Professional Elective I | PE | 3 | 0 | 0 | 3 | 3 |
| 19VL1611 | VLSI Design Laboratory I | PC | 0 | 0 | 4 | 2 | 4 |
| | | **TOTAL** | **18** | **1** | **4** | **21** | **23** |

| **SECOND SEMESTER** | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Code No.** | **Course** | **Category** | **L** | **T** | **P** | **C** | **H** |
| 19VL2601 | Testing of VLSI Circuits | PC | 3 | 0 | 0 | 3 | 3 |
| 19VL2602 | VLSI Signal Processing | PC | 3 | 1 | 0 | 4 | 4 |
| 19VL2603 | Low Power VLSI Design | PC | 3 | 0 | 0 | 3 | 3 |
| | Professional Elective II | PE | 3 | 0 | 0 | 3 | 3 |
| | Professional Elective III | PE | 3 | 0 | 0 | 3 | 3 |
| | Professional Elective IV | PE | 3 | 0 | 0 | 3 | 3 |
| 19VL2611 | VLSI Design Laboratory II | PC | 0 | 0 | 4 | 2 | 4 |
| 19VL2911 | Term Paper Writing | EEC | 0 | 0 | 2 | 1 | 2 |
| | | **TOTAL** | **18** | **1** | **6** | **22** | **25** |

| **THIRD SEMESTER** | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Code No.** | **Course** | **Category** | **L** | **T** | **P** | **C** | **H** |
| | Professional Elective V | PC | 3 | 0 | 0 | 3 | 3 |
| | Professional Elective VI | PE | 3 | 0 | 0 | 3 | 3 |
| | Professional Elective VII | PE | 3 | 0 | 0 | 3 | 3 |
| 19VL3911 | Project Work Phase I | EEC | 0 | 0 | 12 | 6 | 12 |
| | | **TOTAL** | **9** | **0** | **12** | **15** | **21** |

| **FOURTH SEMESTER** | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Code No.** | **Course** | **Category** | **L** | **T** | **P** | **C** | **H** |
| 19VL4911 | Project Work Phase II | EEC | 0 | 0 | 24 | 12 | 24 |
| | | **TOTAL** | **0** | **0** | **24** | **12** | **24** |

| **L - Lecture** | **T-Tutorial** | **P- Practical** | **H- Hours** |
|---|---|---|---|

| **Code No.** | **Course** | **L** | **T** | **P** | **C** |
|---|---|---|---|---|---|
| **PROFESSIONAL ELECTIVES** | | | | | |
| **PROFESSIONAL ELECTIVE I** | | | | | |
| 19VL1701 | Advanced MOSFET Modelling | 3 | 0 | 0 | 3 |
| 19VL1702 | Design of Analog Filters and Signal Conditioning Circuits | 3 | 0 | 0 | 3 |
| 19VL1703 | Advanced Microprocessors and Microcontrollers | 3 | 0 | 0 | 3 |
| 19VL1704 | RF IC Design | 3 | 0 | 0 | 3 |
| **PROFESSIONAL ELECTIVE II** | | | | | |
| 19VL2701 | Advanced Digital Image Processing | 3 | 0 | 0 | 3 |
| 19VL2702 | Embedded System Design | 3 | 0 | 0 | 3 |
| 19VL2703 | DSP Processor Architecture and Programming | 3 | 0 | 0 | 3 |
| 19VL2704 | Solid State Device Modelling and Simulation | 3 | 0 | 0 | 3 |
| **PROFESSIONAL ELECTIVE III** | | | | | |
| 19CU2707 | Electromagnetic Interference and Compatibility | 3 | 0 | 0 | 3 |
| 19VL2705 | Nano Scale Devices | 3 | 0 | 0 | 3 |
| 19VL2706 | FPGA Based System Design | 3 | 0 | 0 | 3 |
| 19VL2707 | Signal Integrity For High Speed Design | 3 | 0 | 0 | 3 |
| **PROFESSIONAL ELECTIVE IV** | | | | | |
| 19VL2708 | MEMS and NEMS | 3 | 0 | 0 | 3 |
| 19VL2709 | Digital Control Engineering | 3 | 0 | 0 | 3 |
| 19VL2710 | VLSI For Wireless Communication | 3 | 0 | 0 | 3 |
| 19CU2710 | RF System Design | 3 | 0 | 0 | 3 |

| Code No. | Course | L | T | P | C |
|---|---|---|---|---|---|
| **PROFESSIONAL ELECTIVE V** | | | | | |
| **19VL3701** | Reconfigurable architectures | 3 | 0 | 0 | 3 |
| 19VL3702 | Analog to Digital Interfaces | 3 | 0 | 0 | 3 |
| 19VL3703 | Physical Design of VLSI Circuits | 3 | 0 | 0 | 3 |
| 19CU3703 | Internet of Things | 3 | 0 | 0 | 3 |
| **PROFESSIONAL ELECTIVE VI** | | | | | |
| 19VL3704 | Network on Chip | 3 | 0 | 0 | 3 |
| 19VL3705 | Electronic Packaging And Testing | 3 | 0 | 0 | 3 |
| 19CU3701 | Soft Computing Techniques | 3 | 0 | 0 | 3 |
| 19CU3705 | Pattern Recognition And Machine Learning | 3 | 0 | 0 | 3 |
| **PROFESSIONAL ELECTIVE VII** | | | | | |
| 19VL3706 | Scripting Language for VLSI | 3 | 0 | 0 | 3 |
| 19VL3707 | Hardware and Software Co Design | 3 | 0 | 0 | 3 |
| 19VL3708 | Selected Topics in IC Design | 3 | 0 | 0 | 3 |
| 19CU3709 | Network Processors | 3 | 0 | 0 | 3 |

## SEMESTER –I

| **FIRST SEMESTER** | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Code No.** | **Course** | **Category** | **L** | **T** | **P** | **C** | **H** |
| 19MA1255 | Advanced Applied Mathematics | ES | 3 | 1 | 0 | 4 | 4 |
| 19VL1601 | Advanced Digital System Design | PC | 3 | 0 | 0 | 3 | 3 |
| 19VL1602 | Analog IC Design | PC | 3 | 0 | 0 | 3 | 3 |
| 19VL1603 | CAD for VLSI circuits | PC | 3 | 0 | 0 | 3 | 3 |
| 19VL1604 | Digital CMOS VLSI Design | PC | 3 | 0 | 0 | 3 | 3 |
| | Professional Elective I | PE | 3 | 0 | 0 | 3 | 3 |
| 19VL1611 | VLSI Design Laboratory I | PC | 0 | 0 | 4 | 2 | 4 |
| | | **TOTAL** | **18** | **1** | **4** | **21** | **23** |

**19MA1255 ADVANCED APPLIED MATHEMATICS L T P C 3 1 0 4**

**OBJECTIVES:**

The main objective of this course is to demonstrate various analytical skills in applied mathematics and extensive experience with the tactics of problem solving and logical thinking applicable in electronics engineering. This course also will help the students to identify, formulate, abstract, and solve problems in electrical engineering using mathematical tools from a variety of mathematical areas, including fuzzy logic, matrix theory, probability, dynamic programming and queuing theory.

**OUTCOMES:**

After completing this course, students should demonstrate competency in the following skills:

- Concepts of fuzzy sets, knowledge representation using fuzzy rules, fuzzy logic, fuzzy prepositions and fuzzy quantifiers and applications of fuzzy logic.
- Apply various methods in matrix theory to solve system of linear equations.
- Computation of probability and moments, standard distributions of discrete and continuous random variables and functions of a random variable.
- Conceptualize the principle of optimality and sub-optimization, formulation and computational procedure of dynamic programming
- Exposing the basic characteristic features of a queuing system and acquire skills in analyzing queuing models.
- Using discrete time Markov chains to model computer systems.

**UNIT I FUZZY LOGIC 12**

Classical logic –Multivalued logics –Fuzzy propositions –Fuzzy quantifiers.

**UNIT II MATRIX THEORY 12**

Some important matrix factorizations –The Cholesky decomposition –QR factorization –Leastsquares method –Singular value decomposition.

**.UNIT III ONE DIMENSIONAL RANDOM VARIABLES 12**

Random variables -Probability function –moments –moment generating functions and their properties – Binomial, Poisson, Geometric, Uniform, Exponential and Normal distributions .

**UNIT IV DYNAMIC PROGRAMMING 12**

Dynamic programming –Principle of optimality –Forward and backward recursion –Applications of dynamic programming –Problem of dimensionality.

**UNIT V QUEUEING MODELS 12**

Poisson Process –Markovian queues –Single and Multi-server Models –Little's formula- Steady State analysis.

**TOTAL PERIODS 60**

**REFERENCES:**

1. George J. Klir and Yuan, B., Fuzzy sets and fuzzy logic, Theory and applications, Prentice Hall of India Pvt. Ltd., 1997.

2. Moon, T.K., Sterling, W.C., Mathematical methods and algorithms for signal processing, Pearson Education, 2000

.3.Richard Johnson, Miller & Freund's Probability and Statistics for Engineers, 7thEdition, Prentice – Hall of India, Private Ltd., New Delhi (2007).

4.Taha, H.A., Operations Research, An introduction, 7thedition, Pearson education editions, Asia, New Delhi, 2002.

5. Donald Gross and Carl M. Harris, Fundamentals of Queuing theory, 2ndedition, John Wiley and Sons, New York (1985)

**19VL1601 ADVANCED DIGITAL SYSTEM DESIGN L T P C 3 0 0 3**

**Course Objectives**

- To introduce methods to analyze and design synchronous and asynchronous sequential
- circuits
- To introduce the architectures of programmable devices
- To introduce design and implementation of digital circuits using programming tools

**Course Outcomes**

1. At the end of the course, the student should be able to:

2. Analyze and design sequential digital circuits
3. Identify the requirements and specifications of the system required for a given application
4. Design and use programming tools for implementing digital circuits of industry standards

**UNIT I SEQUENTIAL CIRCUIT DESIGN 9**

Analysis of clocked synchronous sequential circuits and modelling- State diagram, state table, state table assignment and reduction-Design of synchronous sequential circuits design of iterative circuitsASM chart and realization using ASM

**UNIT II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN 9**

Analysis of asynchronous sequential circuit – flow table reduction-races-state assignment-transition table and problems in transition table- design of asynchronous sequential circuit-Static, dynamic and essential hazards – data synchronizers – mixed operating mode asynchronous circuits – designing vending machine controller

**UNIT III FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS 9**

Fault table method-path sensitization method – Boolean difference method-D algorithm – Tolerance techniques – The compact algorithm – Fault in PLA – Test generation-DFT schemes – Built in self-test

**UNIT IV SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES 9**

Programming logic device families – Designing a synchronous sequential circuit using PLA/PAL Realization of finite state machine using PLD – FPGA – Xilinx FPGA-Xilinx 4000

**UNIT V SYSTEM DESIGN USING VERILOG 9**

Hardware Modelling with Verilog HDL – Logic System, Data Types and Operators For Modelling in Verilog HDL - Behavioural Descriptions in Verilog HDL – HDL Based Synthesis – Synthesis of Finite State Machines– structural modelling – compilation and simulation of Verilog code –Test bench - Realization of combinational and sequential circuits using Verilog – Registers – counters – sequential machine – serial adder – Multiplier- Divider – Design of simple microprocessor

**TOTAL: 45 PERIODS**

**REFERENCES:**

1. Charles H.RothJr “Fundamentals of Logic Design” Thomson Learning 2004

2. M.D.Ciletti ,Modelling, Synthesis and Rapid Prototyping with the Verilog HDL, Prentice Hall, 1999

3. M.G.Arnold, Verilog Digital – Computer Design, Prentice Hall (PTR), 1999.

4. Nripendra N Biswas “Logic Design Theory” Prentice Hall of India,2001

5. ParagK.Lala “Fault Tolerant and Fault Testable Hardware Design” B S. Publications,2002

7. ParagK.Lala “Digital system Design using PLD” B S Publications,2003

8. S. Palnitkar , Verilog HDL – A Guide to Digital Design and Synthesis, Pearson , 2003.

**19VL1602 ANALOG IC DESIGN L T P C 3 0 0 3**

**Course Objectives**

- To study MOS devices modelling and scaling effects.
- To familiarize the design of single stage and multistage MOS amplifier and analysis their frequency responses.
- To study the different design parameters in designing voltage reference and OPAMP circuits.

**Course Outcomes**

- To design MOS single stage, multistage amplifiers and OPAMP for desired frequencies
- Analyze Stability, frequency response, and Noise in MOS amplifiers

**UNIT I MOSFET METRICS 9**

Simple long channel MOSFET theory – SPICE Models – Technology trend, Need for Analog design - Sub-micron transistor theory, Short channel effects, Narrow width effect, Drain induced barrier lowering, Sub-threshold conduction, Reliability, Digital metrics, Analog metrics

**UNIT II SINGLE STAGE AND TWO STAGE AMPLIFIERS 9**

Single Stage Amplifiers – Common source amplifier with resistive load, diode load, constant current load, Source degeneration Source follower, Input and output impedance, Common gate amplifier - Differential Amplifiers – differential and common mode response, Input swing, gain, diode load and constant current load

**UNIT III FREQUENCY RESPONSE OF SINGLE STAGE AND TWO STAGE AMPLIFIERS 9**

Frequency Response of Single Stage Amplifiers – Noise in Single stage Amplifiers – Stability and Frequency Compensation in Single stage Amplifiers, Frequency Response of Two Stage Amplifiers, – Noise in two stage Amplifiers – Stability, gain and phase margins, Frequency Compensation in two stage Amplifiers, Effect of loading in feedback networks,

**UNIT IV CURRENT MIRRORS AND REFERENCE CIRCUITS 9**

Cascode, Negative feedback, Wilson, Regulated cascode, Bandgap voltage reference, Constant Gm biasing, supply and temperature independent reference, curvature compensation, trimming, Effect of transistor mismatch in analog design

**UNIT V OP AMPS 9**

Gilbert cell and applications, Basic two stage OPAMP, two-pole system response, common mode and differential gain, Frequency response of OPAMP, CMFB circuits, slew rate, power supply rejection ratio, random offset, systematic offset, Noise, Output stage, OTA and OPAMP circuits - Low voltage OPAMP **TOTAL : 45 PERIODS**

**REFERENCES:**

1. BehzadRazavi, "Design of Analog CMOS Integrated Circuits", McGraw Hill, 2000
2. Philip E.Allen, "CMOS Analog Circuit Design", Oxford University Press, 2013
3. Paul R.Gray, "Analysis and Design of Analog Integrated Circuits", Wiley Student edition, 5th edition, 2009.
4. R.Jacob Baker, "CMOS: Circuit Design, Layout , and Simulation", Wiley Student Edition, 2009

**19VL1603 CAD FOR VLSI CIRCUITS L T P C 3 0 0 3**

**Course Objectives**

- Learn VLSI Design methodologies
- Understand VLSI design automation tools
- Study modelling and simulation

**Course Outcomes**

1. Understand the flow of VLSI and general purpose algorithms
2. Understand the design rules and implement the Layout with proper placement and partitioning algorithm.
3. Design algorithms to perform Floor planning and Partitioning
4. Understand the Synthesis Simulation process
5. Design algorithms for Assignment and scheduling problems

**UNIT I INTRODUCTION TO VLSI DESIGN FLOW 9**

Introduction to VLSI Design methodologies, Basics of VLSI design automation tools, Algorithmic Graph Theory and Computational Complexity, Tractable and Intractable problems, General purpose methods for combinatorial optimization.

**UNIT II LAYOUT, PLACEMENT AND PARTITIONING 9**

Layout Compaction, Design rules, Problem formulation, Algorithms for constraint graph compaction, Placement and partitioning, Circuit representation, Placement algorithms, Partitioning

**UNIT III FLOOR PLANNING AND ROUTING 9**

Floor planning concepts, Shape functions and floor plan sizing, Types of local routing problems, Area routing, Channel routing, Global routing, Algorithms for global routing.

**UNIT IV SIMULATION AND LOGIC SYNTHESIS 9**

Simulation, Gate-level modelling and simulation, Switch-level modelling and simulation, Combinational Logic Synthesis, Binary Decision Diagrams, Two Level Logic Synthesis.

**UNIT V HIGH LEVEL SYNTHESIS 9**

Hardware models for high level synthesis, internal representation, allocation, assignment and scheduling, scheduling algorithms, Assignment problem, High level transformations.

**TOTAL: 45 PERIODS**

**REFERENCES:**

1. S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons, 2002.
2. Sadiq M. Sait, Habib Youssef, "VLSI Physical Design automation: Theory and Practice", World Scientific 1999.
3. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002.

**19VL1604 DIGITAL CMOS VLSI DESIGN L T P C 3 0 0 3**

**Course Objectives:**

- This course deals comprehensively with all aspects of transistor level design of all the digital building blocks common to all CMOS microprocessors, DPSs, network processors, digital backend of all wireless systems etc.
- The focus will be on the transistor level design and will address all important issues related to size, speed and power consumption.
- The units are classified according to the important building and will introduce the principles and design methodology in terms of the dominant circuit choices, constraints and performance measures.

**Course Outcomes**

1. At the end of the course, the student should be able to:
2. Carry out transistor level design of the most important building blocks used in digital CMOS VLSI circuits.
3. Discuss design methodology of arithmetic building block
4. Analyze trade-offs of the various circuit choices for each of the building block.

**UNIT I MOS TRANSISTOR PRINCIPLES AND CMOS INVERTER 9**

MOS (FET) Transistor Characteristic under Static and Dynamic Conditions, MOS Transistor Secondary Effects, Process Variations, Technology Scaling, Internet Parameter and electrical wise models CMOS Inverter - Static Characteristic, Dynamic Characteristic, Power, Energy, and Energy Delay parameters.

**UNIT II COMBINATIONAL LOGIC CIRCUITS 9**

Propagation Delays, Stick diagram, Layout diagrams, Examples of combinational logic design, Elmore"s constant, Dynamic Logic Gates, Pass Transistor Logic, Power Dissipation, Low Power Design principles.

**UNIT III SEQUENTIAL LOGIC CIRCUITS 9**

Static Latches and Registers, Dynamic Latches and Registers, Timing Issues, Pipelines, Pulse and sense amplifier based Registers, Non bistable Sequential Circuits.

**UNIT IV ARITHMETIC BUILDING BLOCKS AND MEMORY ARCHITECTURES 9**

Data path circuits, Architectures for Adders, Accumulators, Multipliers, Barrel Shifters, Speed and Area Tradeoffs, Memory Architectures, and Memory control circuits.

**UNIT V INTERCONNECT AND CLOCKING STRATEGIES 9**

Interconnect Parameters – Capacitance, Resistance, and Inductance, Electrical Wire Models, Timing classification of Digital Systems, Synchronous Design, Self-Timed Circuit Design.

**TOTAL: 45 PERIODS**

**REFERENCES:**

1. Jan Rabaey, Anantha Chandrakasan, B Nikolic, "Digital Integrated Circuits: A Design Perspective". Second Edition, Feb 2003, Prentice Hall of India.

2. Jacob Baker "CMOS: Circuit Design, Layout, and Simulation, Third Edition", Wiley IEEE Press 2010 3rd Edition.

3. M J Smith, "Application Specific Integrated Circuits", Addisson Wesley, 1997

4. N.Weste, K. Eshraghian, " Principles of CMOS VLSI Design". Second Edition, 1993 Addision Wesley.

**19VL1611 VLSI DESIGN LABORATORY I L T P C 0 0 4 2**

**Course Objectives**

The laboratory based study for the entire program is clubbed under three categories.

- One is the FPGA based design methodology;
- Second is the simulation of analog building blocks, and analog and digital CAD design flow.
- FPGAs are important platform used throughout the industry both in their own right in building complete systems. They are also used as validation/verification platforms prior to undertaking cost and time intensive design and fabrication of custom VLSI designs. Starting from high level design entry in the form VHDL/Verilog codes the students will be carrying out complete hardware level FPGA validation of important digital algorithms. In addition, exercises on the SPICE simulation of the basic CMOS analog building blocks will be carried out.

**TOTAL:45 PERIODS**

**Course Outcomes**

- After completing this course, given a digital system specification, the student should be able to map it onto FPGA platform and carry out a series of validations design starting from design entry to hardware testing. In addition, the student also will be able to design and carry out time

domain and frequency domain simulations of simple analog building blocks, study the pole zero behaviors of feedback based circuits and compute the input/output impedances.

**EXPERIMENTS:**

1. Understanding Synthesis principles. Back annotation.
2. Test vector generation and timing analysis of sequential and combinational logic design realized using HDL languages.
3. FPGA real time programming and I/O interfacing.
4. Interfacing with Memory modules in FPGA Boards.
5. Verification of design functionality implemented in FPGA by capturing the signal in DSO.
6. Real time application development.
7. Design Entry Using VHDL or Verilog examples for Digital circuit descriptions using HDL languages sequential, concurrent statements and structural description.

## SEMESTER II

| **SECOND SEMESTER** | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Code No.** | **Course** | **Category** | **L** | **T** | **P** | **C** | **H** |
| 19VL2601 | Testing of VLSI Circuits | PC | 3 | 0 | 0 | 3 | 3 |
| 19VL2602 | VLSI Signal Processing | PC | 3 | 1 | 0 | 4 | 4 |
| 19VL2603 | Low Power VLSI Design | PC | 3 | 0 | 0 | 3 | 3 |
| | Professional Elective II | PE | 3 | 0 | 0 | 3 | 3 |
| | Professional Elective III | PE | 3 | 0 | 0 | 3 | 3 |
| | Professional Elective IV | PE | 3 | 0 | 0 | 3 | 3 |
| 19VL2611 | VLSI Design Laboratory II | PC | 0 | 0 | 4 | 2 | 4 |
| 19VL2911 | Term Paper Writing | EEC | 0 | 0 | 2 | 1 | 2 |
| | | **TOTAL** | **18** | **1** | **4** | **22** | **25** |

**19VL2601 TESTING OF VLSI CIRCUITS L T P C 3 0 0 3**

**Course Objectives**

- To understand about testing, fault models and types of simulations.
- Learn test generation for sequential and combinational logic circuits
- To design digital VLSI circuits with DFT
- To understand the concepts behind testable design, BIST
- To understand fault diagnosis.

**Course Outcomes**

1. Ability to know about importance of testing and its types in VLSI circuits.

2. Ability to determine fault oriented test vectors for single stuck-at-faults in combinational and Sequential circuits.
3. Prepare design for testability
4. Discuss test algorithms
5. Explain fault diagnosis

**UNIT I FAULT SIMULATION 9**

Introduction to testing – Faults in Digital Circuits – Modelling of faults – Logical Fault Models –Fault detection – Fault Location – Fault dominance – Logic simulation – Types of simulation –Delay models – Gate Level Event – driven simulation.

**UNIT II TEST GENERATION FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS 9**

Test generation for combinational logic circuits – Testable combinational logic circuit design – Test generation for sequential circuits – design of testable sequential circuits.

**UNIT III DESIGN FOR TESTABILITY 9**

Design for Testability – Ad-hoc design – generic scan based design – classical scan based design– system level DFT approaches.

**UNIT IV BUILT IN SELF – TEST AND ALGORITHMS 9**

Built-In self-test – test pattern generation for BIST – Circular BIST – BIST Architectures – Testable Memory Design – Test Algorithms – Test generation for Embedded RAMs.

**UNIT V FAULT DIAGNOSIS 9**

Logical Level Diagnosis – Diagnosis by UUT reduction – Fault Diagnosis for Combinational Circuits– Self-checking design – System Level Diagnosis.

**Total: 45 Periods**

**References:**

1. A.L.Crouch, “Design Test for Digital IC‟s and Embedded Core Systems”, Prentice HallInternational, 2002.
2. M.Abramovici, M.A.Breuer and A.D. Friedman, “Digital systems and Testable Design”, JaicoPublishing House, 2002.
3. M.L.Bushnell and V.D.Agrawal, “Essentials of Electronic Testing for Digital, Memory andMixed- Signal VLSI Circuits”, Kluwer Academic Publishers, 2002.
4. P.K. Lala, “Digital Circuit Testing and Testability”, Academic Press, 2002.

**19VL2602 VLSI SIGNAL PROCESSING L T P C 3 1 0 4**

**Course Objectives**

- To introduce techniques for altering the existing DSP structures to suit VLSI implementations.
- To analyze the various pipelining and parallel processing techniques.

- To analyze the retiming and unfolding algorithms for various DSP applications.
- To introduce efficient design of DSP architectures suitable for VLSI

**Course Outcomes**

1. Ability to modify the existing or new DSP architectures suitable for VLSI.
2. Analyze the concept of pipelining and other processing for DSP applications.
3. Analyze the retiming and unfolding algorithms for various DSP applications.

**UNIT I INTRODUCTION TO DSP SYSTEMS, PIPELINING AND PARALLEL PROCESSING OF FIR FILTERS 12**

Introduction to DSP systems – Typical DSP algorithms, Data flow and Dependence graphs – critical path, Loop bound, iteration bound, Longest path matrix algorithm, Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing for low power.

**UNIT II RETIMING, ALGORITHMIC STRENGTH REDUCTION 12**

Retiming – definitions and properties, Unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application, Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters, Odd-Even merge-sort architecture, parallel rank-order filters.

**UNIT III FAST CONVOLUTION, PIPELINING AND PARALLEL PROCESSING OF IIR FILTERS 12**

Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and parallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with power-of-2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.

**UNIT IV BIT-LEVEL ARITHMETIC ARCHITECTURES 12**

Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, Design of Lyon‟s bit-serial multipliers using Horner‟s rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner‟s rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters

**UNIT V NUMERICAL STRENGTH REDUCTION, SYNCHRONOUS, WAVE AND ASYNCHRONOUS PIPELINING 12**

Numerical strength reduction – sub expression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered single phase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining bundled data versus dual rail protocol.

**Total: 60 Periods**

**References:**

1. Keshab K. Parhi, " VLSI Digital Signal Processing Systems, Design and implementation ", Wiley, Interscience, 2007.
2. U. Meyer – Baese, " Digital Signal Processing with Field Programmable Gate Arrays", Springer, Second Edition, 2004.

**19VL2603 LOW POWER VLSI DESIGN L T P C 3 0 0 3**

**Course Objectives**

- Identify sources of power in an IC.
- Identify the power reduction techniques based on technology independent and technology dependent
- Power dissipation mechanism in various MOS logic style.
- Identify suitable techniques to reduce the power dissipation.
- Design memory circuits with low power dissipation

**Course Outcomes**

1. The student will get to know the basics and advanced techniques in low power design which is a hot topic in today's market where the power plays major role.
2. The reduction in power dissipation by an IC earns a lot including reduction in size, cost and etc.

**UNIT I POWER DISSIPATION IN CMOS 9**

Physics of power dissipation in CMOS FET devices – Hierarchy of limits of power – Sources of power consumption – Static Power Dissipation, Active Power Dissipation - Designing for Low Power, Circuit Techniques For Leakage Power Reduction - Basic principle of low power design.

**UNIT II POWER OPTIMIZATION 9**

Logic level power optimization – Circuit level low power design – Standard Adder Cells, CMOS Adders Architectures-BiCMOS adders - Low Voltage Low Power Design Techniques, Current Mode Adders -Types Of Multiplier Architectures, Braun, Booth and Wallace Tree Multipliers and their performance comparison

**UNIT III DESIGN OF LOW POWER CMOS CIRCUITS 9**

Computer arithmetic techniques for low power system – low voltage low power static Random access and dynamic Random access memories – low power clock, Inter connect and layout design – Advanced techniques – Special techniques.

**UNIT IV POWER ESTIMATION 9**

Power Estimation techniques – logic power estimation – Simulation power analysis –Probabilistic power analysis.

**UNIT V SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER 9**

Synthesis for low power – Behavioral level transform – software design for low power.

**TOTAL: 45 PERIODS**

**References:**

1. AbdelatifBelaouar, Mohamed.I.Elmasry, "Low power digital VLSI design", Kluwer, 1995.

2. A.P.Chandrasekaran and R.W.Broadersen, "Low power digital CMOS design", Kluwer,1995.

3. DimitriosSoudris, C.Pignet, Costas Goutis,"Designing CMOS Circuits for Low Power"Kluwer, 2002.

4. Gary Yeap, "Practical low power digital VLSI design", Kluwer, 1998.

5. James B.Kulo, Shih-Chia Lin, "Low voltage SOI CMOS VLSI devices and Circuits", John Wiley and sons, inc. 2001.

6. J.B.Kulo and J.H Lou, "Low voltage CMOS VLSI Circuits", Wiley 1999.

7. Kaushik Roy and S.C.Prasad, "Low power CMOS VLSI circuit design", Wiley, 2000.

8. Kiat-send Yeo, Kaushik Roy "Low-Voltage, Low-power VLSI Subsystem", Tata McGraw-Hill, 2009

**19VL2611 VLSI DESIGN LABORATORY II L T P C 0 0 4 2**

**Course Objective:**

The focus of this course the CAD based VLSI design flow. The entire VLSI design industry makes use of this design flow in some for or the other. Proficiency and familiarity with the various stages of a typical „state of this design flow is a prerequisite for any student who wishes to be apart of either the industry or their search in VLSI over one full semester exposure to various stages of a typical state of the art CAD VLSI tool be provided by various experiments designed to bring out the key aspects of simulation, and power and clock routing modules. ASIC RTL realization of an available open source MCU.

**Course Outcomes**

The student would have hands on experience in the carrying out a complete VLSI based experiments using / CADENCE/ TANNER/ Mentor/Synopsis

**EXPERIMENTS:**

- To synthesize and understand the Boolean optimization in synthesis.
- Static timing analyses procedures and constraints.
- Critical path considerations. Scan chain insertion, Floor planning, Routing and Placement procedures.
- Power planning, Layout generation, LVS and back annotation,
- Total power estimate. Analog circuit simulation.
- Simulation of logic gates, Current mirrors, Current sources,
- Differential amplifier in Spice. Layout generations, LVS, Back annotation

**TOTAL: 45 PERIODS**

**19VL2911 TERM PAPER WRITING L T P C 0 0 2 1**

In this course, students will develop their scientific and technical reading and writing skills that they need to understand and construct research articles. A term paper requires a student to obtain information from a variety of sources (i.e., Journals, dictionaries, reference books) and then place it in logically developed ideas. The work involves the following steps:

1. Selecting a subject, narrowing the subject into a topic
2. Stating an objective.
3. Collecting the relevant bibliography (at least 15 journal papers)
4. Preparing a working outline.
5. Studying the papers and understanding the author's contributions and critically analysing each paper.
6. Preparing a working outline
7. Linking the papers and preparing a draft of the paper.
8. Preparing conclusions based on the reading of all the papers.
9. Writing the Final Paper and giving final Presentation

Please keep a file where the work carried out by you is maintained.

Activities to be carried out,

| **Activity** | **Instructions** | **Submission week** | **Evaluation** |
|---|---|---|---|
| Selection of area of interest and Topic<br>Stating an Objective | You are requested to select an area of interest, topic and state an objective | 2nd week | **3 %** Based on clarity of thought, current relevance and clarity in writing |
| Collecting Information about your area & topic | 1. List 1 Special Interest Groups or professional society<br>2. List 2 journals<br>3. List 2 conferences, symposia or workshops<br>4. List 1 thesis title<br>5. List 3 web presences (mailing lists, forums, news sites)<br>6. List 3 authors who publish regularly in your area<br>7. Attach a call for papers (CFP) from your area. | 3rd week | **3%** ( the selected information must be area specific and of international and national standard) |

| | | | |
|---|---|---|---|
| Collection of Journal papers in the topic in the context of the objective – collect 20 & then filter | • You have to provide a complete list of references you will be using- Based on your objective - Search various digital libraries and Google Scholar<br>• When picking papers to read - try to:<br>• Pick papers that are related to each other in some ways and/or that are in the same field so that you can write a meaningful survey out of them,<br>• Favour papers from well-known journals and conferences,<br>• Favour "first" or "foundational" papers in the field (as indicated in other people's survey paper),<br>• Favour more recent papers,<br>• Pick a recent survey of the field so you can quickly gain an overview,<br>• Find relationships with respect to each other and to your topic area (classification scheme/categorization)<br>• Mark in the hard copy of papers whether complete work or section/sections of the paper are being considered | 4th week | **6%** ( the list of standard papers and reason for selection) |
| Reading and notes for first 5 papers | Reading Paper Process<br>• For each paper form a Table answering the following questions:<br>• What is the main topic of the article?<br>• What was/were the main issue(s) the author said they want to discuss?<br>• Why did the author claim it was important?<br>• How does the work build on other's work, in the author's opinion?<br>• What simplifying assumptions does the author claim to be making?<br>• What did the author do?<br>• How did the author claim they were going to evaluate their work and Compare it to others? | 5th week | **8%** ( the table given should indicate your understanding of the paper and the evaluation is based on your conclusions about each paper) |

| | | | |
|---|---|---|---|
| | • What did the author say were the limitations of their research?<br>• What did the author say were the important directions for future research?<br>Conclude with limitations/issues not addressed by the paper ( from the perspective of your survey) | | |
| Reading and notes for next5 papers | Repeat Reading Paper Process | 6th week | **8%** ( the table given should indicate your understanding of the paper and the evaluation is based on your conclusions about each paper) |
| Reading and notes for final 5 papers | Repeat Reading Paper Process | 7th week | **8%** ( the table given should indicate your understanding of the paper and the evaluation is based on your conclusions about each paper) |
| Draft outline 1 and Linking papers | Prepare a draft Outline, your survey goals, along with a classification / categorization diagram | 8th week | **8%** ( this component will be evaluated based on the linking and classification among the papers) |
| Abstract | Prepare a draft abstract and give a presentation | 9th week | **6%** (Clarity, purpose and conclusion) **6%** Presentation & Viva Voce |
| Introduction Background | Write an introduction and background sections | 10th week | **5% ( clarity)** |
| Sections of the paper | Write the sections of your paper based on the classification / categorization diagram in keeping with the goals of your survey | 11thweek | **10%** (this component will be evaluated based on the linking and classification among the papers) |
| Your conclusions | Write your conclusions and future work | 12th week | **5%** ( conclusions – clarity and your ideas) |
| Final Draft | Complete the final draft of your paper | 13th week | **10%** (formatting, English, Clarity and linking) **4%** Plagiarism Check Report |
| Seminar | A brief 15 slides on your paper | 14th & 15th week | **10%** (based on presentation and Viva-voce) |

**Total: 30 Periods**

| **THIRD SEMESTER** | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Code No.** | **Course** | **Category** | **L** | **T** | **P** | **C** | **H** |
| | Professional Elective V | PC | 3 | 0 | 0 | 3 | 3 |
| | Professional Elective VI | PE | 3 | 0 | 0 | 3 | 3 |
| | Professional Elective VII | PE | 3 | 0 | 0 | 3 | 3 |
| 19VL3911 | Project Work Phase I | EEC | 0 | 0 | 12 | 6 | 12 |
| | | **TOTAL** | **9** | **0** | **12** | **15** | **21** |

## PROFESSIONAL ELECTIVES

| **PROFESSIONAL ELECTIVE I** | | | | | |
|---|---|---|---|---|---|
| 19VL1701 | Advanced MOSFET Modeling | 3 | 0 | 0 | 3 |
| 19VL1702 | Design of Analog Filters and Signal Conditioning Circuits | 3 | 0 | 0 | 3 |
| 19VL1703 | Advanced Microprocessors and Microcontrollers | 3 | 0 | 0 | 3 |
| 19VL1704 | RF IC Design | 3 | 0 | 0 | 3 |

**19VL1701 ADVANCED MOSFET MODELLING L T P C 3 0 0 3**

**OBJECTIVE:**

The present and future generation VLSI systems are all expected to be built using MOSFETs. Over the years, the VLSI industry has systematically adapted to the use of only MOSFET for all purposes. This is because of its potential from manufacturability point of view. Over the years, advances in physics have given rise many new concepts including carbon nano tubes, organic electronics, single electron and molecular transistors and so on. Even in most of these and other emerging nanotechnology based systems, the MOSFET or devices with MOSFET like characteristics continue to play a very important role. The present course will introduce and cover in detail all the important techniques used for MOSFET device modeling. This course can be considered as an extension or advanced version of the course on „SOLID STATE DEVICE MODELING AND SIMULATION"

**OUTCOMES**:

The student who completes this course will be able to utilize the various MOSFET device models available the various CAD tools, contribute to the development and study of newer models for both existing and emerging newer versions of MOSFET devices

**UNIT I BASIC DEVICE PHYSICS 9**

Intrinsic and extrinsic semiconductors, direct and indirect semiconductors.Electrons and holes in silicon - energy bands, electron and hole densities in equilibrium, Fermi-Dirac statistics, carrier concentration, ionization of impurities. Carrier transport in silicon – drift current, diffusion current. p-n junctions - built-in potential, electric field, current-voltage characteristics.

**UNIT II MOSFET DEVICES 9**

MOS capacitors - surface potential, accumulation, depletion, inversion, electrostatic potential and charge distribution, threshold voltage, polysilicon work function, interface states and oxide traps.Long-channel MOSFETs – threshold voltage, substrate bias and temperature dependence of threshold voltage, drain-current model, sub-threshold characteristics, channel mobility, capacitances.

**UNIT III NANO-SCALED CLASSICAL MOSFETs 9**

Scaling of MOSFETs – constant-voltage scaling, constant-field scaling. Short-channel MOSFETs – short-channel effects, velocity saturation, channel length modulation, source-drain series resistance, DIBL, GIDL. Variability in MOSFETs. Reliability of MOSFETs - high-field effects, hot carrier degradation, negative-bias temperature instability, MOSFET breakdown, high-k dielectrics.

**UNIT IV NON-CLASSICAL MOSFETs 9**

Need for non-classical MOSFETs, Silicon-On-Insulator MOSFETs- Current-voltage equations, fully depleted SOI MOSFETs, partially-depleted SOI MOSFETs, Heterostructure MOSFETs – strained channel MOSFETs, Power MOSFETs - SiC MOSFETs, Silicon Nanowires, Carbon Nanotubes.

**UNIT V COMPACT MODELS FOR CIRCUIT SIMULATORS 9**

Introduction to compact models, SPICE Level - 1, 2 and 3 MOS models, BSIM model, EKV model, PSP model, Noise modelling, High-frequency models, Parameter extraction of MOSFETs.

**TOTAL: 45 PERIODS**

**REFERENCES:**

1. Y. Taur and T. H. Ning, “Fundamentals of Modern VLSI Devices”, Cambridge University Press, Cambridge, United Kingdom.
2. B. G. Streetman and S. Banarjee, “Solid State Electronic Devices”, Prentice-Hall of India Pvt. Ltd, New Delhi, India.
3. N. DasGupta and A. DasGupta, “Semiconductor Devices – Modeling and Technology”, Prentice-Hall of India Pvt. Ltd, New Delhi, India.
4. B. Bhattacharyya, “Compact MOSFET Models for VLSI Design”, John Wiley & Sons Inc., 2009.
5. K. Maiti, N. B. Chakrabarti, S. K. Ray, "Strained silicon heterostructures: materials and devices”, The Institution of Electrical Engineers, London, United Kingdom.

**19VL1702 DESIGN OF ANALOG FILTERS AND SIGNAL CONDITIONING CIRCUITS**

**L T P C 3 0 0 3**

**Course Objectives**

- This course deals with CMOS circuit design of various Analog Filter architectures.
- The required signal conditioning techniques in a Mixed signal IC environment are also dealt in this course.

**Course Outcomes**

1. The student will apply the operational and design principles for all the important active analog filter configurations.
2. The student also will gain working knowledge of signal conditioning techniques and the necessary guide lines in a Mixed signal IC environment.

**UNIT I FILTER TOPOLOGIES 9**

The Bilinear Transfer Function - Active RC Implementation, Transconductor-C Implementation, Switched Capacitor Implementation, Biquadratic Transfer Function, Active RC implementation, Switched capacitor implementation, High Q, Q peaking and instability, Transconductor-C Implementation, the Digital Biquad.

**UNIT II INTEGRATOR REALIZATION 9**

Low pass Filters, Active RC Integrators – Effect of finite Op-Amp Gain Bandwidth Product, Active RC SNR, gm-C Integrators, Discrete Time Integrators.

**UNIT III SWITCHED CAPACITOR FILTER REALIZATION 9**

Switched capacitor Technique, Biquadratic SC Filters, SC N-path filters, Finite gain and bandwidth effects, Layout consideration, Noise in SC Filters.

**UNIT IV SIGNAL CONDITIONING TECHNIQUES 9**

Interference types and reduction, Signal circuit grounding, Shield grounding, Signal conditioners for capacitive sensors, Noise and Drift in Resistors, Layout Techniques.

**UNIT V SIGNAL CONDITIONING CIRCUITS 9**

Isolation Amplifiers, Chopper and Low Drift Amplifiers, Electrometer and Transimpedance Amplifiers, Charge Amplifiers, Noise in Amplifiers

**TOTAL : 45 PERIODS**

**References:**

1. Ramson Pallas-Areny, John G. Webster “Sensors and Signal Conditioning” , A wiley Inter science Publication, John Wiley & Sons INC,2001.
2. R.Jacob Baker, ”CMOS Mixed-Signal Circuit Design”, John Wiley & Sons, 2008.

3. Schauman, Xiao and Van Valkenburg, "Design of Analog Filters", Oxford University Press, 2009

**19VL1703 ADVANCED MICROPROCESSORS AND MICROCONTROLLERS L T P C 3 0 0 3**

**Course Objectives**

1. To study 80386 and Pentium processor.
2. To understand CISC and RISC Architectures.
3. To Learn ARM processor.

**Course Outcomes**

1. Discuss 80386 and Pentium Processor.
2. Introduction to RISC architectures.
3. Discuss the register and memory management system of ARM processor.
4. Outline ARM instruction set and addressing modes.
5. Explain PIC microcontroller and motorola 68HC11 microcontroller.

**UNIT I 80386 AND PENTIUM PROCESSOR 9**

80386 PROCESSOR: Basic programming model – Memory organization – Data types – Instruction set - Addressing mode – Address translation – Interrupts –PENTIUM PROCESSOR: Introduction to Pentium processor architecture – Special Pentium Registers – Pentium Memory Management – Introduction to Pentium pro processor – Pentium Pro Special Features.

**UNIT II CISC and RISC Architecture 9**

Introduction to RISC architectures: RISC Versus CISC – RISC Case studies: MIPS R4000 – SPARC – Intel i860 - IBM RS/6000.

**UNIT III ARM PROCESSOR 9**

ARM Programmer"s Model – Registers – Processor Modes – State of the processor – Condition Flags – ARM Pipelines – Exception Vector Table – ARM Processor Families – Typical 3 stage pipelined ARM organization–Introduction to ARM Memory Management Unit.

**UNIT IV ARM ADDRESSING MODES AND INSTRUCTION SET 9**

ARM Addressing Modes – ARM Instruction Set Overview – Thumb Instruction Set Overview – LPC210X ARM Processor Features.

**UNIT V PIC MICROCONTROLLER AND MOTOROLA 68HC11 MICROCONTROLLER 9**

Instruction set, addressing modes – operating modes- Interrupt system- RTC-Serial Communication Interface – A/D Converter PWM and UART. MOTOROLA: CPU Architecture – Instruction set – interrupts- Timers- I 2C Interfacing –UART- A/D Converter – PWM

**Total: 45 Periods**

**References:**

1. Andrew Sloss, "ARM System Developer‟s Guide", Morgan Kaufmann Publishers, 2005.
2. Barry B Brey, "The Intel Microprocessor, Pentium and Pentium Pro Processor, Architecture Programming and Interfacing", Prentice Hall of India, 2002.
3. Daniel Tabak, "Advanced Microprocessors", McGraw Hill Inc., 1995.
4. David E Simon "An Embedded Software Primer", Pearson Education, 2007.
5. Gene .H.Miller ." Micro Computer Engineering ," Pearson Education , 2003.
6. Intel, "Microprocessors, Vol-I &Vol-II", Intel Corporation, USA, 1992.
7. John .B.Peatman , " Design with PIC Microcontroller , Prentice hall, 1997.
8. Mohammed Rafiquzzaman, "Microprocessors and Microcomputer Based System Design", Universal Book Stall, New Delhi, 1990.
9. Steve Furber, "ARM System-on-Chip Architecture", Pearson Education, 2005 "ARM7 TDMI Technical Reference Manual", ARM Ltd., UK, 2004 6.

**19VL1704 RF IC DESIGN L T P C 3 0 0 3**

**Course Objectives**

- To study the various impedance matching techniques used in RF circuit design.
- To understand the functional design aspects of LNAs, Mixers, PLLs and VCO.
- To understand frequency synthesis.

**Course Outcomes**

1. To understand the principles of operation of an RF receiver front end and be able to design and apply constraints for LNAs, Mixers and Frequency synthesizers

**UNIT I IMPEDANCE MATCHING IN AMPLIFIERS 9**

Definition of „Q", serie parallel transformations of lossy circuits, impedance matching using „L", „PI"and T networks, Integrated inductors, resistors, Capacitors, tunable inductors, transformers

**UNIT II AMPLIFIER DESIGN 9**

Noise characteristics of MOS devices, Design of CG LNA and inductor degenerated LNAs.

Principles of RF Power Amplifiers design,

**UNIT III ACTIVE AND PASSIVE MIXERS 9**

Qualitative Description of the Gilbert Mixer - Conversion Gain, and distortion and noise , analysis of Gilbert Mixer – Switching Mixer - Distortion in Unbalanced Switching Mixer -Conversion Gain in Unbalanced Switching Mixer - Noise in Unbalanced Switching Mixer - A Practical Unbalanced Switching Mixer. Sampling Mixer - Conversion Gain in Single Ended Sampling Mixer - Distortion in Single Ended Sampling Mixer - Intrinsic Noise in Single Ended Sampling Mixer - Extrinsic Noise in Single Ended Sampling Mixer.

**UNIT IV OSCILLATORS 9**

LC Oscillators, Voltage Controlled Oscillators, Ring oscillators, Delay Cells, tuning range in ring oscillators, Tuning in LC oscillators, Tuning sensitivity, Phase Noise in oscillators, sources of phase noise

**UNIT V PLL AND FREQUENCY SYNTHESIZERS 9**

Phase Detector/Charge Pump, Analog Phase Detectors, Digital Phase Detectors, Frequency Dividers, Loop Filter Design, Phase Locked Loops, Phase noise in PLL, Loop Bandwidth, Basic Integer-N frequency synthesizer, Basic Fractional-N frequency synthesizer

**Total: 45 Periods**

**References:**

**1. B**.Razavi ,"RF Microelectronics" , Prentice-Hall ,1998

2. Bosco H Leung "VLSI for Wireless Communication", Pearson Education, 2002

3. BehzadRazavi, "Design of Analog CMOS Integrated Circuits" McGraw-Hill, 1999

4. Jia-sheng Hong, "Microstrip filters for RF/Microwave applications", Wiley, 2001

5. Thomas H.Lee, "The Design of CMOS Radio –Frequency Integrated Circuits", Cambridge University Press ,2003

| **PROFESSIONAL ELECTIVE II** | | | | | |
|---|---|---|---|---|---|
| 19VL2701 | Advanced Digital Image Processing | 3 | 0 | 0 | 3 |
| 19VL2702 | Embedded System Design | 3 | 0 | 0 | 3 |
| 19VL2703 | DSP Processor Architecture and Programming | 3 | 0 | 0 | 3 |
| 19VL2704 | Solid State Device Modelling and Simulation | 3 | 0 | 0 | 3 |

**19VL2701 ADVANCED DIGITAL IMAGE PROCESSING L T P C 3 0 0 3**

**Course Objectives**:

1. To understand the image fundamentals.
2. To understand the various image segmentation techniques.
3. To extract features for image analysis.
4. To introduce the concepts of image registration and image fusion.
5. To illustrate 3D image visualization.

**Course Outcomes**:

Upon Completion of the course, the students will be able to

1. Explain the fundamentals digital image processing.
2. Describe image various segmentation and feature extraction techniques for image analysis.
3. Discuss the concepts of image registration and fusion.

4. Explain 3D image visualization.

**UNIT I FUNDAMENTALS OF DIGITAL IMAGE PROCESSING 9**

Elements of visual perception, brightness, contrast, hue, saturation, mach band effect, 2D image transforms-DFT, DCT, KLT, SVD. Image enhancement in spatial and frequency domain, Review of Morphological image processing.

**UNIT II SEGMENTATION 9**

Edge detection, Thresholding, Region growing, Fuzzy clustering, Watershed algorithm, Active contour models, Texture feature based segmentation, Graph based segmentation, Wavelet based Segmentation - Applications of image segmentation.

**UNIT III FEATURE EXTRACTION 9**

First and second order edge detection operators, Phase congruency, Localized feature extraction - detecting image curvature, shape features, Hough transform, shape skeletonization, Boundary descriptors, Moments, Texture descriptors- Autocorrelation, Co-occurrence features, Runlength features, Fractal model based features, Gabor filter, wavelet features.

**UNIT IV REGISTRATION AND IMAGE FUSION 9**

Registration - Preprocessing, Feature selection - points, lines, regions and templates Feature correspondence - Point pattern matching, Line matching, Region matching, Template matching. Transformation functions - Similarity transformation and Affine Transformation. Resampling – Nearest Neighbour and Cubic Splines. Image Fusion - Overview of image fusion, pixel fusion, wavelet based fusion -region based fusion.

**UNIT V 3D IMAGE VISUALIZATION 9**

Sources of 3D Data sets, Slicing the Data set, Arbitrary section planes, The use of color, Volumetric display, Stereo Viewing, Ray tracing, Reflection, Surfaces, Multiple connected surfaces, Image processing in 3D, Measurements on 3D images.

**TOTAL: 45 PERIODS**

**REFERENCES:**

1. ArdeshirGoshtasby, " 2D and 3D Image registration for Medical, Remote Sensing and Industrial Applications",John Wiley and Sons,2005.
2. Anil K. Jain, Fundamentals of Digital Image Processing', Pearson Education, Inc., 2002.
3. John C.Russ, "The Image Processing Handbook", CRC Press,2007.
4. Mark Nixon, Alberto Aguado, "Feature Extraction and Image Processing", Academic Press,2008.
5. Rafael C. Gonzalez, Richard E. Woods, Digital Image Processing', Pearson,Education, Inc.,Second Edition, 2004.

6. Rick S.Blum, Zheng Liu, "Multisensor image fusion and its Applications", Taylor& Francis, 2006.

**19VL2702 EMBEDDED SYSTEM DESIGN L T P C 3 0 0 3**

**Course Objectives**

1. To enable the students to basics of embedded System Design process
2. To understand the flow of control to various I//O devices
3. To understand the programming in embedded systems
4. To study the concept of assembly and C programming for Embedded System
5. To understand the Embedded program and software development process

**Course Outcomes**

1. Revise computing platform and design analysis
2. Demonstrate the working of Embedded processors
3. Discuss the embedded software and program development process

**UNIT I INTRODUCTION TO EMBEDDED PROCESSORS 9**

Embedded Computers, Characteristics of Embedded Computing Applications, and Challenges in Embedded Computing system design. Embedded system design process – Requirements, Specifications, Architecture Design, Designing hardware and software components, System integration

**UNIT II EMBEDDED PROCESSOR & COMPUTING PLATFORM 9**

Data operations, Flow of control, SHARC processor – Memory organization, Data operations, Flow of control, Parallelism with instructions, CPU Bus Configuration, ARM Bus, SHARC bus, Memory devices, input/output devices, Component interfacing, Designing with microprocessor development and debugging.

**UNIT III PROGRAMMING EMBEDDED SYSTEMS 9**

Embedded Program – Role of Infinite loop – Compiling, Linking and locating – downloading and debugging – Emulators and simulators processor – External peripherals – Types of memory – Memory testing – Flash Memory.

**UNIT IV C ANDASSEMBLY 9**

Overview of Embedded C - Compilers and Optimization - Programming and Assembly – Register usage conventions – typical use of addressing options – instruction sequencing – procedure call and return – parameter passing – retrieving parameters – everything in pass by value – temporary variables.

**UNIT V EMBEDDED PROGRAM AND SOFTWARE DEVELOPMENT PROCESS 9**

Program Elements – Queues – Stack- List and ordered lists-Embedded programming in C++ - Inline Functions and Inline Assembly - Portability Issues - Embedded Java- Software Development process:

Analysis – Design Implementation – Testing – Validation- Debugging - Software maintenance.

**Total: 45 Periods**

**Text Book:**

1. W. Wolf, "Computers as Components: Principles of Embedded Computing Systems Design", Morgan Kaufman Publisher, 2001, ISBN 1-55860-541-x (case), ISBN 1-55860-693-9 (paper).

**References:**

1. Daniel W. lewis "Fundamentals of Embedded Software where C and Assembly meet" PHI 2002.
2. Raj Kamal, "Embedded Systems- Architecture, Programming and Design" Tata McGraw Hill, 2006.
3. F. Wahid, "Embedded System Design" John Wiley & Sons publisher. ISBN – 13, 9789971514051, ISBN – 9971514052, (Paper)
4. K.V.K.K.Prasad, "Embedded Real-Time Systems: Concepts, Design & Programming", dreamtech press, 2005
5. David E-Simon, "An Embedded Software Primer", Pearson Education, 2007.

**19VL2703 DSP PROCESSOR ARCHITECTURE AND PROGRAMMING L T P C 3 0 0 3**

**Course Objectives**

The objective of this course is to provide in-depth knowledge on

- Digital Signal Processor basics
- Third generation DSP Architecture and programming skills
- Advanced DSP architectures and some applications.

**Course Outcomes**

Students should be able to:

- Become Digital Signal Processor specialized engineer
- DSP based System Developer

**UNIT I FUNDAMENTALS OF PROGRAMMABLE DSPs 9**

Multiplier and Multiplier accumulator – Modified Bus Structures and Memory access in PDSPs – Multiple access memory – Multi-port memory – VLIW architecture- Pipelining – Special Addressing modes in P-DSPs – On chip Peripherals.

**UNIT II TMS320C5X PROCESSOR 9**

Architecture – Assembly language syntax - Addressing modes – Assembly language Instructions - Pipeline structure, Operation – Block Diagram of DSP starter kit – Application Programs for processing real time signals.

**UNIT III TMS320C6X PROCESSOR 9**

Architecture of the C6x Processor - Instruction Set - DSP Development System: Introduction – DSP Starter Kit Support Tools- Code Composer Studio - Support Files - Programming Examples to Test the DSK Tools – Application Programs for processing real time signals.

**UNIT IV ADSP PROCESSORS 9**

Architecture of ADSP-21XX and ADSP-210XX series of DSP processors- Addressing modes and assembly language instructions – Application programs –Filter design, FFT calculation.

**UNIT V ADVANCED PROCESSORS 9**

Architecture of TMS320C54X: Pipe line operation, Code Composer studio – Architecture of TMS320C6X - Architecture of Motorola DSP563XX – Comparison of the features of DSP family processors.

**TOTAL: 45 PERIODS**

**References:**

1. Avtar Singh and S. Srinivasan, Digital Signal Processing – Implementations using DSP Microprocessors with Examples from TMS320C54xx, cengage Learning India Private Limited, Delhi 2012

2. B.Venkataramani and M.Bhaskar, "Digital Signal Processors – Architecture, Programming and Applications" – Tata McGraw – Hill Publishing Company Limited. New Delhi, 2003.

3. RulphChassaing, Digital Signal Processing and Applications with the C6713 and C6416 DSK, A John Wiley & Sons, Inc., Publication, 2005

4. User guides Texas Instrumentation, Analog Devices, Motorola.

**19VL2704 SOLID STATE DEVICE MODELLING AND SIMULATION L T P C 3 0 0 3**

**OBJECTIVE:**

- To acquaint the students with fundamentals of building device and circuit simulators, and efficient use of simulators.

**UNIT I MOSFET DEVICE PHYSICS 9**

MOSFET capacitor, Basic operation, Basic modelling,Advanced MOSFET modelling, RF modelling of MOS transistors, Equivalent circuit representation of MOS transistor, Highfrequencybehavior of MOS transistor and A.C small signal modelling, model parameterextraction, modelling parasitic BJT, Resistors, Capacitors, Inductors.

**UNIT II DEVICE MODELLING 9**

Prime importance of circuit and device simulations in VLSI; Nodal, mesh, modified nodal and

hybrid analysis equations. Solution of network equations:Sparse matrix techniques, solution of nonlinear networks through Newton-Raphson technique, convergence and stability.

**UNIT III MULTISTEP METHODS 9**

Solution of stiff systems of equations, adaptation of multistep methods to the solution of electrical networks, general purpose circuit simulators.

**UNIT IV MATHEMATICAL TECHNIQUES FOR DEVICE SIMULATIONS 9**

Poisson equation, continuity equation, drift-diffusion equation, Schrodinger equation, hydrodynamic equations, trap rate, finite difference solutions to these equations in 1D and 2D space, grid generation.

**UNIT V SIMULATION OF DEVICES** 9

Computation of characteristics of simple devices like p-n junction, MOS capacitor and MOSFET; Small-signal analysis.

**References**

1. Arora, N., "MOSFET Models for VLSI Circuit Simulation", Springer-Verlag, 1993
2. Selberherr, S., "Analysis and Simulation of Semiconductor Devices", Springer-Verlag., 1984
3. Fjeldly, T., Yetterdal, T. and Shur, M., "Introduction to Device Modeling and Circuit Simulation", Wiley-Interscience., 1997
4. Grasser, T., "Advanced Device Modeling and Simulation", World Scientific Publishing Company., 2003
5. Chua, L.O. and Lin, P.M., "Computer-Aided Analysis of Electronic Circuits: Algorithms and Computational Techniques", Prentice-Hall., 1975
6. TrondYtterdal, Yuhua Cheng and Tor A. FjeldlyWayne Wolf, "Device Modeling for Analog and RF CMOS Circuit Design", John Wiley & Sons Ltd

| **PROFESSIONAL ELECTIVE III** | | | | | |
|---|---|---|---|---|---|
| 19CU2707 | Electromagnetic Interference and Compatibility | 3 | 0 | 0 | 3 |
| 19VL2705 | Nano Scale Devices | 3 | 0 | 0 | 3 |
| 19VL2706 | FPGA Based System Design | 3 | 0 | 0 | 3 |
| 19VL2707 | Signal Integrity For High Speed Design | 3 | 0 | 0 | 3 |

**19CU2707 ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY L T P C 3 0 0 3**

**Course Objectives**

The basics of EMI

1. EMI sources.
2. EMI problems.
3. Solution methods in PCB.
4. Measurements techniques for emission.

**Course Outcomes**

1. Identify Standards
2. Understand various coupling mechanism
3. Discuss EMI mitigation techniques
4. Analyse Various standards and regulations
5. Compare EMI test methods

**UNIT I BASIC THEORY 9**

Introduction to EMI and EMC, Intra and inter system EMI, Elements of Interference, Sources and Victims of EMI, Conducted and Radiated EMI emission and susceptibility, Case Histories, Radiation hazards to humans, Various issues of EMC, EMC Testing categories EMC Engineering Application.

**UNIT II COUPLING MECHANISM 9**

Electromagnetic field sources and Coupling paths, Coupling via the supply network, Common mode coupling, Differential mode coupling, Impedance coupling, Inductive and Capacitive coupling,Radioactive coupling, Ground loop coupling, Cable related emissions and coupling, Transient sources, Automotive transients.

**UNIT III EMI MITIGATION TECHNIQUES 9**

Working principle of Shielding and Murphy‟s Law, LF Magnetic shielding, Apertures and shielding effectiveness, Choice of Materials for H, E, and free space fields, Gasketting and sealing, PCB Level

shielding, Principle of Grounding, Isolated grounds, Grounding strategies for Large systems, Grounding for mixed signal systems, Filter types and operation, Surge protection devices, Transient Protection.

**UNIT IV STANDARD AND REGULATION 9**

Need for Standards, Generic/General Standards for Residential and Industrial environment, BasicStandards, Product Standards, National and International EMI Standardizing Organizations; IEC, ANSI, FCC, AS/NZS, CISPR, BSI, CENELEC, ACEC. Electro Magnetic Emission and susceptibility standards and specifications, MIL461E Standards.

**UNIT V EMI TEST METHODS AND INSTRUMENTATION 9**

Fundamental considerations, EMI Shielding effectiveness tests, Open field test, TEM cell for immunity test, Shielded chamber , Shielded anechoic chamber, EMI test receivers, Spectrum analyzer, EMI test wave simulators, EMI coupling networks, Line impedance stabilization networks, Feed through capacitors, Antennas, Current probes, MIL -STD test methods, Civilian STD test methods.

**REFERENCES:**

1. Bemhard Keiser, "Principles of Electromagnetic Compatibility", 3 Ed, Artech house, Norwood, 1986.
2. Clayton Paul, "Introduction to Electromagnetic Compatibility", Wiley Interscience, 2006.
3. Daryl Gerke and William Kimmel, "EDN"s Designer"s Guide to Electromagnetic Compatibility",Elsevier Science & Technology Books, 2002
4. Dr Kenneth L Kaiser, "The Electromagnetic Compatibility Handbook", CRC Press 2005.
5. Electromagnetic Compatibility by Norman Violette ,Published by Springer, 2013
6. Henry W. Ott, "Electromagnetic Compatibility Engineering", John Wiley & Sons Inc, Newyork,2009
7. V Prasad Kodali, "Engineering Electromagnetic Compatibility", IEEE Press, Newyork, 2001.

W Scott Bennett, "Control and Measurement of Unintentional Electromagnetic Radiation", John Wiley & Sons Inc., (Wiley Interscience Series) 1997

**19VL2705 NANO SCALE DEVICES L T P C 3 0 0 3**

**Course Objectives**

- To introduce novel MOSFET devices and understand the advantages of multi-gate devices
- To introduce the concepts of nanoscale MOS transistor and their performance characteristics
- To study the various nano scaled MOS transistors

**Course Outcomes**

- To design circuits using nano scaled MOS transistors with the physical insight of their functional characteristics

**UNIT I INTRODUCTION TO NOVEL MOSFETS 9**

MOSFET scaling, short channel effects - channel engineering - source/drain engineering - high k dielectric - copper interconnects - strain engineering, SOI MOSFET, multigate transistors – single gate – double gate – triple gate – surround gate, quantum effects – volume inversion – mobility – threshold voltage – inter subband scattering, multigate technology – mobility – gate stack

**UNIT II PHYSICS OF MULTIGATE MOS SYSTEMS 9**

MOS Electrostatics – 1D – 2D MOS Electrostatics, MOSFET Current-Voltage Characteristics – CMOS Technology – Ultimate limits, double gate MOS system – gate voltage effect - semiconductor thickness effect – asymmetry effect – oxide thickness effect – electron tunnel current – two dimensional confinement, scattering – mobility

**UNIT III NANOWIRE FETS AND TRANSISTORS AT THE MOLECULAR SCALE 9**

Silicon nanowire MOSFETs – Evaluation of I-V characteristics – The I-V characteristics for non-degenerate carrier statistics – The I-V characteristics for degenerate carrier statistics – Carbon nanotube – Band structure of carbon nanotube – Band structure of graphene – Physical structure of nanotube – Band structure of nanotube – Carbon nanotube FETs – Carbon nanotube MOSFETs – Schottky barrier carbon nanotube FETs – Electronic conduction in molecules – General model for ballistic nano transistors – MOSFETs with 0D, 1D, and 2D channels – Molecular transistors – Single electron charging – Single electron transistors

**UNIT IV RADIATION EFFECTS 9**

Radiation effects in SOI MOSFETs, total ionizing dose effects – single gate SOI – multigate devices, single event effect, scaling effects

**UNIT V CIRCUIT DESIGN USING MULTIGATE DEVICES 9**

Digital circuits – impact of device performance on digital circuits – leakage performance trade off – multi VT devices and circuits – SRAM design, analog circuit design – transconductance - intrinsic gain – flicker noise – self heating –band gap voltage reference – operational amplifier – comparator designs, mixed signal – successive approximation DAC, RF circuits.

**TOTAL : 45 PERIODS**

**References:**

1. J P Colinge, "FINFETs and other multi-gate transistors", Springer – Series on integrated circuits and systems, 2008
2. Mark Lundstrom, Jing Guo, "Nanoscale Transistors: Device Physics, Modeling and Simulation", Springer, 2006
3. M S Lundstorm, "Fundamentals of Carrier Transport"**,** 2nd Ed., Cambridge University Press, Cambridge UK, 2000

**19VL2706 FPGA BASED SYSTEM DESIGN L T P C 3 0 0 3**

**Course Objectives**

1. Learn FPGA Fundamentals
2. Understand FPGA Implementation automation tools
3. Study Architecting Speed, Area, Power
4. Study FPGA Circuits and Design

**Course Outcomes**

1. Understand the flow of FPGA Fundamentals
2. Understand the design rules and FPGA Implementation automation tools.
3. Design algorithms to perform Architecting Speed, Area, Power
4. Design algorithms for FPGA Circuits and Design

**UNIT I FPGA FUNDAMENTALS 9**

Introduction to ASICs and FPGAs, Fundamentals in Digital IC design, FPGA and CPLD architectures, FPGA development board hardware and I/O features, FPGA programming technologies, FPGA logic cell structures, FPGA programmable interconnect and I/O ports, Downloading design to FPGA board, NiosII Processor software development, Nios II Hardware design

**UNIT II FPGA IMPLEMENTATION 9**

FPGA implementation of Combinational circuits, Sequential design and hierarchy, FPGA implementation of sequential circuits, Timing issues in FPGA synchronous circuits, FPGA core library functions, Verilog HDL, Design flow using Verilog HDL, Using Verilog HDL for synthesis of hardware

**UNIT III ARCHITECTING SPEED, AREA, POWER 9**

Architecting speed, Architecting area, architecting power, high level design, Clock domains, Design examples: AES, I2S vs. SPDIF, State machine design: The electric train controller,

**UNIT IV FPGA CIRCUITS 9**

Arithmetic circuits, Implementing Math functions, Example design: FPU, DSP applications, Reset circuits, Coding for synthesis, direct digital frequency synthesiser implementation, Example design: Secure Hash algorithm, synthesis optimization, VGA display using FPGA, Interfacing PS/2 Keyboard and mouse, Digital I/O interfacing standards

**UNIT V FPGA DESIGN 9**

FPGA Microprocessor design, Design of SDRAM controller, Design of half tone pixel converter, Design of ADSL modem, Design of Software Radio, RISC design: Synthesis of MIPS core, Programming FPGA in electronics systems, dynamically reconfigurable systems, Operating system support for SoPC design

***REFERENCES***

1. Wayne Wolf, "FPGA-Based System Design",Prentice Hall, 2004
2. Steve Kilts, "Advanced FPGA Design", Wiley, 2004
3. James O. Hamblen, et.al., "Rapid prototyping of digital systems", Springer- SOPC Edition, 2008

**19VL2707 SIGNAL INTEGRITY FOR HIGH SPEED DESIGN L T P C 3 0 0 3**

**Course Objectives**

- To identify sources affecting the speed of digital circuits.
- To introduce methods to improve the signal transmission characteristics

**Course Outcomes**

1. Ability to identify sources affecting the speed of digital circuits.
2. Able to improve the signal transmission characteristics.

**UNIT I SIGNAL PROPAGATION ON TRANSMISSION LINES 9**

Transmission line equations, wave solution, wave vs. circuits, initial wave, delay time, Characteristic impedance , wave propagation, reflection, and bounce diagrams Reactive terminations – L, C , static field maps of micro strip and strip line cross-sections, per unit length parameters, PCB layer stackups and layer/Cu thicknesses, cross-sectional analysis tools, Zo and Td equations for microstrip and stripline Reflection and terminations for logic gates, fan-out, logic switching , input impedance into a transmission-line section, reflection coefficient, skin-effect, dispersion.

**UNIT II MULTI-CONDUCTOR TRANSMISSION LINES AND CROSS-TALK 9**

Multi-conductor transmission-lines, coupling physics, per unit length parameters ,Near and far-end cross-talk, minimizing cross-talk (stripline and microstrip) Differential signalling, termination, balancedcircuits ,S-parameters, Lossy and Lossles models.

**UNIT III NON-IDEAL EFFECTS `9**

Non-ideal signal return paths – gaps, BGA fields, via transitions , Parasitic inductance and capacitance , Transmission line losses – Rs, tanδ , routing parasitic, Common-mode current, differential-mode current , Connectors

**UNIT IV POWER CONSIDERATIONS AND SYSTEM DESIGN 9**

SSN/SSO , DC power bus design , layer stack up, SMT decoupling ,, Logic families, power consumption, and system power delivery , Logic families and speed Package types and

parasitic,SPICE, IBIS models ,Bit streams, PRBS and filtering functions of link-path components , Eyediagrams , jitter , inter-symbol interference Bit-error rate ,Timing analysis

**UNIT V CLOCK DISTRIBUTION AND CLOCK OSCILLATORS 9**

Timing margin, Clock slew, low impedance drivers, terminations, Delay Adjustments, canceling parasitic capacitance, Clock jitter.

**Total: 45 Periods**

**References**:

1. Douglas Brooks, Signal Integrity Issues and Printed Circuit Board Design, Prentice HallPTR, 2003.
2. Eric Bogatin , Signal Integrity – Simplified , Prentice Hall PTR, 2003.
3. H. W. Johnson and M. Graham, High-Speed Digital Design: A Handbook of Black Magic, Prentice Hall, 1993.
4. S. Hall, G. Hall, and J. McCall, High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices, Wiley-Interscience, 2000.

| **PROFESSIONAL ELECTIVE IV** | | | | | |
|---|---|---|---|---|---|
| 19VL2708 | MEMS and NEMS | 3 | 0 | 0 | 3 |
| 19VL2709 | Digital Control Engineering | 3 | 0 | 0 | 3 |
| 19VL2710 | VLSI For Wireless Communication | 3 | 0 | 0 | 3 |
| 19CU2710 | RF System Design | 3 | 0 | 0 | 3 |

**19VL2708 MEMS AND NEMS L T P C 3 0 0 3**

**Course Objectives**

- To introduce the concepts of micro electromechanical devices.
- To know the fabrication process of Microsystems.
- To know the design concepts of micro sensors and micro actuators.
- To familiarize concepts of quantum mechanics and nano systems.

**Course Outcomes**

1. At the end of this course, the student should be able to:
2. Discuss micro sensors
3. Explain micro actuators
4. Outline nano systems and Quantum mechanics

**UNIT I OVERVIEW** 9

New trends in Engineering and Science: Micro and Nanoscale systems, Introduction to Design of MEMS and NEMS, MEMS and NEMS – Applications, Devices and structures. Materials for MEMS:Silicon, silicon compounds, polymers, metals.

**UNIT II MEMS FABRICATION TECHNOLOGIES** 9

Microsystem fabrication processes: Photolithography, Ion Implantation, Diffusion, Oxidation. Thin film depositions: LPCVD, Sputtering, Evaporation, Electroplating; Etching techniques: Dry and wet etching, electrochemical etching; Micromachining: Bulk Micromachining, Surface Micromachining, High Aspect- Ratio (LIGA and LIGA-like) Technology; Packaging: Microsystems packaging, Essential packaging technologies, Selection of packaging materials

**UNIT III MICRO SENSORS** 9

MEMS Sensors: Design of Acoustic wave sensors, resonant sensor, Vibratory gyroscope, Capacitive and Piezo Resistive Pressure sensors- engineering mechanics behind these Micro sensors. Case study: Piezo-resistive pressure sensor.

**UNIT IV MICRO ACTUATORS** 9

Design of Actuators: Actuation using thermal forces, Actuation using shape memory Alloys, Actuation using piezoelectric crystals, Actuation using Electrostatic forces (Parallel plate, Torsion bar, Comb drive actuators), Micromechanical Motors and pumps. Case study: Comb drive actuators.

**UNIT V NANOSYSTEMS AND QUANTUM MECHANICS 9**

Atomic Structures and Quantum Mechanics, Molecular and Nanostructure Dynamics: Schrodinger Equation and Wave function Theory, Density Functional Theory, Nanostructures and Molecular Dynamics, Electromagnetic Fields and their quantization, Molecular Wires and Molecular Circuits.

**TOTAL: 45 PERIODS**

**REFERENCES:**

1. Chang Liu, “Foundations of MEMS”, Pearson education India limited, 2006.
2. Marc Madou, “Fundamentals of Micro fabrication”, CRC press 1997.
3. Stephen D. Senturia,” Micro system Design”, Kluwer Academic Publishers,2001
4. Sergey Edward Lyshevski, “MEMS and NEMS: Systems, Devices, and Structures” CRC Press, 2002.
5. Tai Ran Hsu ,”MEMS and Microsystems Design and Manufacture” ,Tata Mcraw Hill, 2002.

**19VL2709 DIGITAL CONTROL ENGINEERING L T P C 3 0 0 3**

**Course Objectives**

- The student learns the principles of PI,PD,PID controllers.

- The student analyses time and frequency response discrete time control system.
- The student is familiar with digital control algorithms.
- The student has the knowledge to implement PID control algorithms.

**Course Objective**

1. Describe continuous time and discrete time controllers analytically.
2. Define and state basic analog to digital and digital to analog conversion principles.
3. Analyze sampled data control system in time and frequency domains.
4. Design simple PI, PD, PID continuous and digital controllers.
5. Develop schemes for practical implementation of temperature and motor control systems

**UNIT I CONTROLLERS IN FEEDBACK SYSTEMS 9**

Review of frequency and time response analysis and specifications of first order and second order

feedback control systems, need for controllers, continuous time compensations, continuous time PI,PD, PID controllers, digital PID controllers**.**

**UNIT II BASIC DIGITAL SIGNAL PROCESSING IN CONTROL SYSTEMS 9**

Sampling theorem, quantization, aliasing and quantization error, hold operation, mathematical model of sample and hold, zero and first order hold, factors limiting the choice of sampling rate**,**reconstruction.

**UNIT III MODELLING OF SAMPLED DATA CONTROL SYSTEM 9**

Difference equation description, Z-transform method of description, pulse transfer function, time and frequency response of discrete time control systems, stability of digital control systems, Jury's stability test, state space description, first companion, second companion, Jordan canonical models, discrete state variable models (elementary principles only).

**UNIT IV DESIGN OF DIGITAL CONTROL ALGORITHMS 9**

Review of principle of compensator design, Z-plane specifications, digital compensator design using frequency response plots, discrete integrator, discrete differentiator, development of digital PID controller, transfer function, design in the Z-plane.

**UNIT V PRACTICAL ASPECTS OF DIGITAL CONTROL ALGORITHMS 9**

Algorithm development of PID control algorithms, standard programmes for microcontroller implementation, finite word length effects, choice of data acquisition systems, microcontroller based temperature control systems, microcontroller based motor speed control systems, DSP implementation of motor control system.

**TOTAL: 45 PERIODS**

**References:**

1. John J. D'Azzo, "Constantive Houpios, Linear Control System Analysis and Design", McGraw Hill,1995.

2. Kenneth J. Ayala, "The 8051 Microcontroller- Architecture, Programming and Applications", Penram International, 2nd Edition, 1996.

3. M.Gopal, "Digital Control and Static Variable Methods", Tata McGraw Hill, New Delhi, 1997.

**19VL2710 VLSI FOR WIRELESS COMMUNICATION LT P C 3 0 0 3**

**Course Objectives**:

- To study the design concepts of low noise amplifiers.
- To study the various types of mixers designed for wireless communication
- To study and design PLL and VCO.
- To understand the concepts of CDMA in wireless communication.

**UNIT I COMPONENTS AND DEVICES 9**

Integrated inductors, resistors, MOSFET and BJT AMPLIFIER DESIGN: Low Noise Amplifier Design -Wideband LNA -Design Narrowband LNA -Impedance Matching -Automatic Gain Control Amplifiers –Power Amplifiers

**UNIT II MIXERS 9**

Balancing Mixer -Qualitative Description of the Gilbert Mixer -Conversion Gain –Distortion -Low Frequency Case: Analysis of Gilbert Mixer –Distortion -High-Frequency Case –Noise -A Complete Active Mixer.Switching Mixer -Distortion in Unbalanced Switching Mixer -Conversion Gain in Unbalanced Switching Mixer -Noise in Unbalanced Switching Mixer -A Practical Unbalanced Switching Mixer.Sampling Mixer -Conversion Gain in Single Ended Sampling Mixer -Distortion in Single Ended Sampling Mixer -Intrinsic Noise in Single Ended Sampling Mixer -Extrinsic Noise in Single Ended Sampling Mixer.

**UNIT III FREQUENCY SYNTHESIZERS 9**

Phase Locked Loops -Voltage Controlled Oscillators -Phase Detector –Analog Phase Detectors – Digital Phase Detectors -Frequency Dividers -LC Oscillators -Ring Oscillators -Phase Noise -A Complete Synthesizer Design Example (DECT Application).

**UNIT IV SUB SYSTEMS 9**

Data converters in communications, adaptive Filters, equalizers and transceivers

**UNIT V IMPLEMENTATIONS** 9

VLSI architecture for Multitier Wireless System -Hardware Design Issues for a Next generation CDMA System

**Total Periods: 45**

**REFERENCES**:

1.B.Razavi ,"RF Microelectronics" , Prentice-Hall ,1998.

2.Bosco H Leung "VLSI for Wireless Communication", Pearson Education, 2002.

3.ThomasH.Lee, "The Design of CMOS Radio –Frequency Integrated Circuits', Cambridge University Press ,2003.

4.Emad N Farag and Mohamed I Elmasry, "Mixed Signal VLSI Wireless Design -Circuits and Systems", Kluwer Academic Publishers, 2000.

5.Behzad Razavi, "Design of Analog CMOS Integrated Circuits" McGraw-Hill, 1999.6.J. Crols and M.Steyaert, "CMOS Design," Boston, Kluwer Academic Pub., 1997.

**19CU2710 RF SYSTEM DESIGN L T P C 3 0 0 3**

**Course Objective**

- To understand the fundamentals of RF design and Microwave integrated circuits
- To understand the various components of RF system for Wireless Communications.
- To know the basic techniques needed for analysis of RF systems.

**Course Outcomes**

- Capability to design RF circuits.
- To be able to analyze RF circuits

**UNIT I CMOS PHYSICS, TRANSCEIVER SPECIFICATIONS, ARCHITECTURES 9**

CMOS , Noise: Thermal, shot, flicker, popcorn noise transceiver Specifications: Two port Noise theory, Noise Figure, THD, IP2, IP3, Sensitivity, SFDR, Phase noise. Transceiver Architectures: Receiver: Homodyne, Heterodyne, Image reject, Low IF Architectures, Transmitter: Direct up conversion, Two step up conversion schemes

**UNIT II IMPEDANCE MATCHING AND AMPLIFIERS 9**

Review of S-parameters and Smith chart, Passive IC components, Impedance matching networks, Amplifiers**:** Common Gate, Common Source Amplifiers, OC Time constants in bandwidth estimation and enhancement , High frequency amplifier design, Low Noise Amplifiers: Power match and Noise match , Single ended and Differential schemes.

**UNIT III FEEDBACK SYSTEMS AND POWER AMPLIFIERS 9**

Feedback Systems: Stability of feedback systems: Gain and phase margin, Root-locus techniques, Time and Frequency domain considerations , Compensation Power Amplifiers: General model – Class A,

AB, B, C, D, E and F amplifiers, Linearization Techniques, Efficiency boosting techniques, ACPR metric, Design considerations

**UNIT IV RF FILTER,OSCILLATOR AND MIXER 9**

Overview-basic resonator and filter configuration, special filter realizations, filter implementation. Basic oscillator model, high frequency oscillator configuration, basic characteristics of mixers, phase locked loops, RF directional couplers, hybrid couplers, detector and demodulator circuits.

**UNIT V MIC COMPONENTS 9**

Introduction to MICs, Fabrication Technology, Advantages and applications, MIC components- Micro strip components, Coplanar circuits: Transistors, switches, active filters. Coplanar microwave amplifiers: LNA design and Medium power amplifiers.

**Total: 45 Periods**

**References:**

1.Razavi, "RF Microelectronics", Pearson Education, 1997.

2.Ingo Wolff," Coplanar Microwave Integrated circuits", John Wiley and sons, New Jersey, 2006.

3.T. Lee,"Design of CMOS RF Integrated Circuits", Cambridge, 2004

| **PROFESSIONAL ELECTIVE V** | | | | | |
|---|---|---|---|---|---|
| **19VL3701** | Reconfigurable architectures | 3 | 0 | 0 | 3 |
| 19VL3702 | Analog to Digital Interfaces | 3 | 0 | 0 | 3 |
| 19VL3703 | Physical Design of VLSI Circuits | 3 | 0 | 0 | 3 |
| 19CU3703 | Internet of Things | 3 | 0 | 0 | 3 |

**19VL3701 RECONFIGURABLE ARCHITECTURES L T P C 3 0 0 3**

**Course Objectives**:

The students should be made to:

- Understand concept of reconfigurable systems
- Learn programmed FPGAs
- Study flexibility on routability

**Course Outcomes**

At the end of this course, the students should be able to:

- Compare FPGA routing architectures
- Discuss FPGA applications
- Explain high level synthesis

**UNIT I INTRODUCTION 9**

Domain-specific processors, Application specific processors, Reconfigurable Computing Systems – Evolution of reconfigurable systems – Characteristics of RCS advantages and issues. Fundamental concepts& Design steps –classification of reconfigurable architecture-fine, coarse grain & hybrid architectures – Examples

**UNIT II FPGA TECHNOLOGIES & ARCHITECTURE 9**

Technology trends- Programming technology- SRAM programmed FPGAs, antifuse programmed FPGAs, erasable programmable logic devices. Alternative FPGA architectures: Mux Vs LUT based logic blocks – CLB Vs LAB Vs Slices- Fast carry chains- Embedded RAMs- FPGA Vs ASIC design styles.

**UNIT III ROUTING FOR FPGAS 9**

General Strategy for routing in FPGAs- routing for row-based FPGAs – segmented channel routing, definitions- Algorithm for I segment and K segment routing – Routing for symmetrical FPGAs, Flexibility of FPGA Routing Architectures: FPGA architectural flexibility on Routability- Effect of switch block flexibility on routability - Tradeoffs in flexibility of S and C blocks

**NIT IV HIGH LEVEL DESIGN 9**

FPGA Design style: Technology independent optimization- technology mapping- Placement. Highlevel synthesis of reconfigurable hardware, high- level languages, Design tools: Simulation (cyclebased, event driven based) – Synthesis (logic/HDL vs physically aware) – timing analysis (static vs dynamic)- verification physical design tools.

**UNIT V APPLICATION DEVELOPMENT WITH FPGAS 9**

Case Studies of FPGA Applications–System on a Programmable Chip (SoPC) Designs.

**TOTAL : 45 PERIODS**

**REFERENCES:**

1. Christophe Bobda, "Introduction to Reconfigurable Computing –Architectures, Algorithms and Applications", Springer, 2010.

2. Clive "Max" Maxfield, "The Design Warrior"s Guide to FPGAs: Devices, Tools And Flows", Newnes, Elsevier, 2006.

3. Jorgen Staunstrup, Wayne Wlf, "Hardware/Software Co- Design: Priciples and practice", Kluwer Academic Pub, 1997.

4. Maya B. Gokhale and Paul S. Graham, "Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays", Springer, 2005.

5. Russell tessier and Wayne Burleson "Reconfigurable Computing for Digital Signal Processing: A Survey" Journal of VLSI Signal processing 28,p7-27,2001.

6. Stephen M. Trimberger, "field – programmable Gate Array Technology" Springer,2007.

7. Stephen D. broen, Robert J. Francis, Jonathan Rose, Zvonko G. Vranesic," Fieldprogrammable Gate Arrays", Kluwer Academic Pubnlishers, 1992.

8. Scott Hauck and Andre Dehon (Eds.), "Reconfigurable Computing –The Theory and Practice of FPGA-Based Computation", Elsevier / Morgan Kaufmann, 2008

**19VL3702 ANALOG TO DIGITAL INTERFACES L T P C 3 0 0 3**

**Course objectives**

- To understand the importance of sampling the input analog signal for digitization and enabling
- circuit architectures
- To understand the principles of Analog to Digital and Digital to Analog conversion of signals.
- To understand the importance of calibration techniques for achieving precision during data
- conversion

**Course Outcomes**

- To be able to design Analog to Digital and Digital to Analog data converters based on data precision requirements

**UNIT I SAMPLE AND HOLD CIRCUITS 9**

Sampling switches, Conventional open loop and closed loop sample and hold architecture, Open loop architecture with miller compensation, multiplexed input architectures, recycling architecture switched capacitor architecture.

**UNIT II SWITCHED CAPACITOR CIRCUITS AND COMPARATORS 9**

Switched-capacitor amplifiers, switched capacitor integrator, switched capacitor common mode feedback. Single stage amplifier as comparator, cascaded amplifier stages as comparator, latched comparators.

**UNIT III DIGITAL TO ANALOG CONVERSION 9**

Performance metrics, reference multiplication and division, switching and logic functions in DAC, Resistor ladder DAC architecture, current steering DAC architecture.

**UNIT IV ANALOG TO DIGITAL CONVERSION 9**

Performance metric, Flash architecture, Pipelined Architecture, Successive approximation architecture, Time interleaved architecture.

**UNIT V PRECISION TECHNIQUES 9**

Comparator offset cancellation, Op Amp offset cancellation, Calibration techniques, range overlap and digital correction.

**Total Periods: 45**

**REFERENCE:**

1. Behzad Razavi, "Principles of data conversion system design", S. Chand and company Ltd,

**19VL3703 PHYSICAL DESIGN OF VLSI CIRCUITS L T P C 3 0 0 3**

**Course Objectives**

1. Learn VLSI Technology
2. Understand VLSI Routing and Layout
3. Study Cell Generation And Compaction

**Course Outcomes**

1. Understand the flow of VLSI Technology
2. Understand the design rules and implement the Placement Using Top-Down Approach.
3. Design algorithms to perform Routing Using Top Down Approach
4. Understand the Synthesis Simulation process Circuit Layout
5. Design algorithms for Assignment and Cell Generation and Compaction problems

**UNIT I INTRODUCTION TO VLSI TECHNOLOGY 9**

Layout Rules-Circuit abstraction Cell generation using programmable logic array transistor chaining, Wein-Berger arrays and gate matrices-layout of standard cells gate arrays and sea of gates, field

programmable gate array(FPGA)-layout methodologies-Packaging-Computational Complexity-Algorithmic Paradigms

**UNIT II PLACEMENT USING TOP-DOWN APPROACH 9**

Partitioning: Approximation of Hyper Graphs with Graphs, Kernighan-Lin Heuristic- Ratio-cut-partition with capacity and i/o constraints; Floor planning: Rectangular dual floor planning- hierarchical approach- simulated annealing- Floor plan sizing; Placement: Cost function- force directed method-placement by simulated annealing- partitioning placement- module placement on a resistive network – regular placement- linear placement

**UNIT III ROUTING USING TOP DOWN APPROACH 9**

Fundamentals: Maze running- line searching- Steiner trees; Global Routing: Sequential Approaches-hierarchical approaches- multi-commodity flow based techniques- Randomised Routing- One Step approach- Integer Linear Programming; Detailed Routing: Channel Routing- Switch box routing; Routing in FPGA: Array based FPGA- Row based FPGAs

**UNIT IV PERFORMANCE ISSUES IN CIRCUIT LAYOUT 9**

Delay Models: Gate Delay Models- Models for interconnected Delay- Delay in RC trees. Timing – Driven Placement: Zero Stack Algorithm- Weight based placement- Linear Programming Approach Timing Driving Routing: Delay Minimization- Click Skew Problem- Buffered Clock Trees. Minimization: constrained via Minimization- unconstrained via Minimization- Other issues in minimization

**UNIT V SINGLE LAYER ROUTING, CELL GENERATION AND COMPACTION 9**

Planar subset problem (PSP) - Single layer global routing- Single Layer Global Routing- Single Layer detailed Routing- Wire length and bend minimization technique – Over the Cell (OTC) Routing-Multiple chip modules (MCM) - Programmable Logic Arrays- Transistor chaining- Wein-Burger Arrays- Gate matrix layout- 1D compaction- 2D compaction

**Total Periods: 45**

***REFERENCES***

1. Sarafzadeh, C.K. Wong, “An Introduction to VLSI Physical Design”, McGraw Hill, 1995
2. Preas M. Lorenzatti, “Physical Design and Automation of VLSI systems”, Benjamin Cummins Publishers, 1998
3. Ban Wong, et.al. , “Nano CMOS Circuit and Physical Design” Wiley 2004
4. N.A. Sherwani, “Algorithms for VLSI Physical Design Automation”, Kluwer Academic, 2002
5. Sadiq M. Sait, Habib Youssef, “VLSI Physical Design Automation, Theory and Practice” World Scientific Publishing Company, 2003
6. Bryan T. Preas, “Physical Design Automation of VLSI system”, Benjamin Cummins Publishers, 1998

Erik Brunvand, “Digital VLSI Chip Design with Cadence and Synopsys CAD Tools”, Pearson, 2010

**19CU3703 INTERNET OF THINGS L T P C 3 0 0 3**

**Course Objectives:**

To understand the fundamentals of Internet of Things

- To learn about the basics of IOT protocols
- To build a small low cost embedded system using Raspberry Pi.
- To apply the concept of Internet of Things in the real world scenario

**Course Outcomes**

**Upon completion of the course, the student should be able to:**

1. Analyze various protocols for IoT
2. Develop web services to access/control IoT devices.
3. Design a portable IoT using Rasperry Pi
4. Deploy an IoT application and connect to the cloud.
5. Analyze applications of IoT in real time scenario

**UNIT I INTRODUCTION TO IoT 9**

Internet of Things - Physical Design- Logical Design- IoT Enabling Technologies - IoT Levels & Deployment Templates - Domain Specific IoTs - IoT and M2M - IoT System Management with NETCONF-YANG- IoT Platforms Design Methodology

**UNIT II IoT ARCHITECTURE 9**

M2M high-level ETSI architecture - IETF architecture for IoT - OGC architecture - IoT reference model - Domain model - information model - functional model - communication model - IoT reference architecture

**UNIT III IoT PROTOCOLS 9**

Protocol Standardization for IoT – Efforts – M2M and WSN Protocols – SCADA and RFID Protocols – Unified Data Standards – Protocols – IEEE 802.15.4 – BACNet Protocol – Modbus– Zigbee Architecture – Network layer – 6LowPAN - CoAP - Security

**UNIT IV BUILDING IoT WITH RASPBERRY PI & ARDUINO 9**

Building IOT with RASPERRY PI- IoT Systems - Logical Design using Python – IoT Physical Devices & Endpoints - IoT Device -Building blocks -Raspberry Pi -Board - Linux on Raspberry Pi - Raspberry Pi Interfaces -Programming Raspberry Pi with Python - Other IoT Platforms - Arduino

**UNIT V CASE STUDIES AND REAL-WORLD APPLICATIONS 9**

Real world design constraints - Applications - Asset management, Industrial automation, smart grid, Commercial building automation, Smart cities - participatory sensing - Data Analytics for IoT – Software & Management Tools for IoT Cloud Storage Models & Communication APIs - Cloud for IoT - Amazon Web Services for IoT.

**Total: 45 Periods**

**References**

1. ArshdeepBahga, Vijay Madisetti, “Internet of Things – A hands-on approach”, Universities Press, 2015

2. Dieter Uckelmann, Mark Harrison, Michahelles, Florian (Eds), "Architecting the Internet of Things", Springer, 2011
3. Honbo Zhou, "The Internet of Things in the Cloud: A Middleware Perspective", CRC Press, 2012
4. Jan Ho¨ ller, VlasiosTsiatsis , Catherine Mulligan, Stamatis , Karnouskos, Stefan Avesand. David Boyle, "From Machine-to-Machine to the Internet of Things - Introduction to a New Age of Intelligence", Elsevier, 2014.
5. Olivier Hersent, David Boswarthick, Omar Elloumi , "The Internet of Things – Key applications and Protocols", Wiley, 2012.

| **PROFESSIONAL ELECTIVE VI** | | | | | |
|---|---|---|---|---|---|
| 19VL3704 | Network on Chip | 3 | 0 | 0 | 3 |
| 19VL3705 | Electronic Packaging And Testing | 3 | 0 | 0 | 3 |
| 19CU3701 | Soft Computing Techniques | 3 | 0 | 0 | 3 |
| 19CU3705 | Pattern Recognition And Machine Learning | 3 | 0 | 0 | 3 |

**19VL3704 NETWORK ON CHIP L T P C 3 0 0 3**

**Course Objectives**

1. To understand the fundamentals of 3D NOC.
2. To impart knowledge about testing and energy issues in NOC.
3. To understand the router architectures in 3D NOC.

**Course Outcomes**

1. The ability to understand the need for 3D NOC.
2. The ability to know the concepts used in testing and reduction of power in NOC.
3. The ability to learn the architecture and working of routers in 3D NOC

**UNIT I INTRODUCTION TO THREE DIMENSIONAL NOC 9**

Three-Dimensional Networks-on-Chips Architectures.–Resource Allocation for QoSOn-Chip Communication–Networks-on-Chip Protocols-On-Chip Processor Traffic Modeling for Networks-onChip.

**UNIT II TEST AND FAULT TOLERANCE OF NOC 9**

Design-Security in Networks-on-Chips-Formal Verification of Communications in Networks-onChips-Test and Fault Tolerance for Networks-on-Chip Infrastructures- Monitoring Services for Networks-on-Chips.

**UNIT III ENERGY AND POWER ISSUES OF NOC 9**

Energy and Power Issues in Networks-on-Chips-The CHAIN works Tool Suite: A Complete Industrial Design Flow for Networks-on-Chips

**UNIT IV MICRO-ARCHITECTURE OF NOC ROUTER 9**

Baseline NoC Architecture – MICRO-Architecture Exploration ViChaR: A Dynamic Virtual Channel Regulator for NoC Routers- RoCo: The Row-Column Decoupled Router – A Gracefully Degrading and Energy-Efficient Modular Router Architecture for On-Chip Networks. Exploring Fault Tolerant Networks-on-Chip Architectures.

**UNIT V DimDE ROUTER FOR 3D NOC 9**

A Novel Dimensionally-Decomposed Router for On-Chip Communication in 3D Architectures Digest of Additional NoC MACRO-Architectural Research.

**Total: 45 Periods**

**References**

1. ChrysostomosNicopoulos, Vijaykrishnan Narayanan, Chita R.Das, Networks-on- Chip Architectures AHolistic Design Exploration, Springer,2009.
2. Fayezgebali, Haythamelmiligi, HqhahedWatheq E1-Kharashi, Networks-on-Chips theory and practice, CRC press, 2009.
3. Axel Jantsch ,HannuTenhunen,Networkson Chip, Publisher: Springer; Soft cover reprint of hardcover 1st ed. 2003 edition (November 5, 2010).
4. Giovanni De Micheli , Luca Benini, Networkson Chips: Technology and Tools (Systems on Silicon), Publisher: Morgan Kaufmann; 1 edition (August 3, 2006).
5. Jose Flich ,DavideBertozzi ,Designing Network On-Chip Architectures in the Nanoscale Era, (Chapman Hall/CRC Computational Science), Publisher: Chapman and Hall/CRC; 1 edition (December 18,2010).

**19VL3705 ELECTRONIC PACKAGING AND TESTING L T P C 3 0 0 3**

**Course Objective:**

- To Introduce and Discuss Various Issues Related To The System Packaging

## Course Outcome

At the end of the course, the student should be able to:

- Give a comprehensive introduction to the various packaging types used along with the associated thermal, speed, signal and integrity power issues
- Enable design of packages which can withstand higher temperature, vibrations and shock
- Design of PCBs which minimize the EMI and operate at higher frequency

- Analyze the concepts of Testing and testing method

**UNIT I OVERVIEW OF ELECTRONIC SYSTEMS PACKAGING 9**

Functions of an Electronic Package, Packaging Hierarchy, IC packaging: MEMS packaging, consumer electronics packaging, medical electronics packaging, Trends, Challenges, Driving Forces on Packaging Technology, Materials for Microelectronic packaging, Packaging Material Properties, Ceramics, Polymers, and Metals in Packaging, Material for high density interconnect substrates

**UNIT II ELECTRICAL ISSUES IN PACKAGING 9**

Electrical Issues of Systems Packaging, Signal Distribution, Power Distribution, Electromagnetic Interference, Transmission Lines, Clock Distribution, Noise Sources, Digital and RF Issues. Design Process Electrical Design: Interconnect Capacitance, Resistance and Inductance fundamentals; Packaging roadmaps -Hybrid circuits -Resistive, Capacitive and Inductive parasitic

**UNIT III CHIP PACKAGES 9**

IC Assembly -Purpose, Requirements, Technologies, Wire bonding, Tape Automated Bonding, Flip Chip, Wafer Level Packaging, reliability, wafer level burn –in and test. Single chip packaging: functions, types, materials processes, properties, characteristics, trends. Multi chip packaging: types, design, comparison, trends. System –in -package (SIP); Passives: discrete, integrated, and embedded

**UNIT IV PCB, SURFACE MOUNT TECHNOLOGY AND THERMAL CONSIDERATIONS 9**

Printed Circuit Board: Anatomy, CAD tools for PCB design, Standard fabrication, Micro via Boards. Board Assembly: Surface Mount Technology, Through Hole Technology, Process Control and Design challenges.Thermal Management, Heat transfer fundamentals, Thermal conductivity and resistance, Conduction, convection and radiation –Cooling requirements

**UNIT V TESTING 9**

Reliability, Basic concepts, Environmental interactions. Thermal mismatch and fatigue –failures – thermo mechanically induced –electrically induced –chemically induced. Electrical Testing: System level electrical testing, Interconnection tests, Active Circuit Testing, Design for Testability

**Total: 45 Periods**

**REFERENCES:**

1.Tummala, Rao R., Fundamentals of Microsystems Packaging, McGraw Hill, 2001:1.Blackwell (Ed), The electronic packaging handbook, CRC Press, 2000.

2.Tummala, Rao R, Microelectronics packaging handbook, McGraw Hill, 2008.

3.Bosshart, Printed Circuit Boards Design and Technology, TataMcGraw Hill, 1988.

4.R.G. Kaduskar and V.B.Baru, Electronic Product design, Wiley India, 2011

5.R.S.Khandpur, Printed Circuit Board, Tata McGraw Hill, 2005.

6.Recent literature in Electronic Packaging

7.Michael L. Bushnell &Vishwani D. Agrawal,‖ Essentials of Electronic Testing for Digital, memory & Mixed signal VLSI Circuits‖, Kluwer Academic Publishers.2000

.8.M. Abramovici, M. A. Breuer, and A.D. Friedman, ―Digital System Testing and Testable Design‖, Computer Science Press,1990

**19CU3701 SOFT COMPUTING TECHNIQUES L T P C 3 0 0 3**

**OBJECTIVES**

To know the basics of artificial neural networks

1. To provide adequate knowledge about feed forward /feedback neural networks
2. To apply the concept of fuzzy logic in various systems.
3. To have the idea about genetic algorithm
4. To provide adequate knowledge about the applications of Soft Computing.

**OUTCOMES:**

1. Knowledge on concepts of soft computational techniques.
2. Able to apply soft computational techniques to solve various problems.
3 .Motivate to solve research oriented problems

**UNIT I ARTIFICIAL NEURAL NETWORK 9**

Introduction-Basic concepts of Neural Network-Model of an Artificial Neuron-Characteristics of Neural Network-Learning Methods-Back propagation Network Architecture-Back propagation Learning-Counter Propagation Network-Hopfield/Recurrent Network-Adaptive Resonance Theory

**UNIT II FUZZY LOGIC 9**

Basic concepts of Fuzzy Logic-Fuzzy Sets and Crisp Sets-Fuzzy Set Theory and Operations-Properties of Fuzzy Sets-Fuzzy and Crisp relations, Fuzzy to Crisp Conversion-Membership Functions-Interference in Fuzzy Logic-Fuzzy if-then Rules, Fuzzy implications and Fuzzy Algorithms, Fuzzification & Defuzzification-Fuzzy Controller

**UNIT III NEURO-FUZZY MODELLING 9**

ANFIS Architecture-Classification and Regression Trees-Data Clustering algorithms-Rulebase Structure Identification.

**UNIT IV GENETIC ALGORITHMS 9**

Basic concepts-Working Principle-Inheritance Operators-Cross Over-Inversion & Deletion-Mutation Operator-Generation Cycle.

**UNIT V APPLICATIONS OF SOFTCOMPUTING 9**

Genetic Algorithm Application- Bagley and Adaptive Game-Playing Program- Greg Viols Fuzzy Cruise Controller-Air Conditioner Controller-Application of Back Propagation Neural Network

**Total: 45 Periods**

**REFERENCES**

1. George J. Klir and Bo Yuan, „Fuzzy Sets and Fuzzy Logic Theory and Applications‟, Prentice Hall of India, 2002

2. J.S.R.Jang,C.T.Sun and E.Mizutani,"Neuro-Fuzzy and Soft Computing",PHI,2004, Pearson Education 2004.

3. LaureneFausett,"Fundamentals of Neural Networks: Architectures, Algorithms and Applications", Pearson Education India, 2006.

4. S.Rajasekaran and G.A.V.Pai."Neural Networks, Fuzzy Logic and Genetic Algorithms", PHI, 2010.

5. Timothy J Ross, "Fuzzy logic with Engineering Applications", John Wiley and Sons, 2009.

**6.** Zimmermann H.J."Fuzzy Set Theory and Its Application" Springer International

**19CU3705 PATTERN RECOGNITION AND MACHINE LEARNING L T P C 3 0 0 3**

**Course Objectives:**

- Study the fundamental of pattern classifier.
- To know about various clustering concepts.
- To originate the various structural pattern recognition and feature extraction.
- To understand the basic of concept learning and decision trees
- To explore recent advances in pattern recognition.

**Course Objectives**

**Upon Completion of the course, the students will be able to**

- Classify the data and identify the patterns.
- Utilize the given data set to extract and select features for Pattern recognition.

  Describe the decision tree and concept learning.
- Discuss on recent advances in pattern recognition

**UNIT I PATTERN CLASSIFIER 9**

Overview of Pattern recognition – Discriminant functions – Supervised learning –Parametric estimation – Maximum Likelihood Estimation – Bayesian parameter Estimation – Problems with Bayes approach– Pattern classification by distance functions –Minimum distance pattern classifier.

**UNIT II CLUSTERING 9**

Clustering for unsupervised learning and classification -Clustering concept – C-means algorithm – Hierarchical clustering procedures -Graph theoretic approach to pattern clustering -Validity of clusters.

**UNIT III FEATURE EXTRACTION AND STRUCTURAL PATTERN RECOGNITION 9** KL Transforms – Feature selection through functional approximation – Binary selection -Elements of formal grammars - Syntactic description - Stochastic grammars –Structural representation.

**UNIT IV INTRODUCTION, CONCEPT LEARNING AND DECISION TREES 9**

Learning Problems – Designing Learning systems, Perspectives and Issues – Concept Learning – Version Spaces and Candidate Elimination Algorithm – Inductive bias – Decision Tree learning – Representation – Algorithm – Heuristic Space Search

**UNIT V EVOLUTIONARY AND GRAPHICAL MODELS** 9

– Evolutionary Learning – Genetic algorithms – Genetic Offspring: - Genetic Operators – Using Genetic Algorithms – Reinforcement Learning – Overview – Getting Lost Example – Markov Decision Process , Markov Chain Monte Carlo Methods – Sampling – Proposal Distribution – Markov Chain Monte Carlo – Graphical Models – Bayesian Networks – Markov Random Fields – Hidden Markov Models – Tracking Methods

**Total: 45 Periods**

**REFERENCES:**

1. Duda R.O., and Hart.P.E., Pattern Classification and Scene Analysis, Wiley, New York, 1973.

2. Morton Nadier and Eric Smith P., Pattern Recognition Engineering, John Wiley & Sons, New York, 1993.

3. NarasimhaMurty M and Susheela Devi V, "Pattern Recognition – An Algorithmic Approach", Springer, Universities Press, 2011

4. Robert J.Schalkoff, Pattern Recognition : Statistical, Structural and Neural Approaches, John Wiley &Sons Inc., New York, 2007.

5. Tom M. Mitchell, "Machine Learning", McGraw-Hill Education (Indian Edition), 2013.

6. Tou and Gonzalez, Pattern Recognition Principles, Wesley Publication Company, London

| **PROFESSIONAL ELECTIVE VII** | | | | | |
|---|---|---|---|---|---|
| 19VL3706 | Scripting Language for VLSI | 3 | 0 | 0 | 3 |
| 19VL3707 | Hardware and Software Co Design | 3 | 0 | 0 | 3 |
| 19VL3708 | Selected Topics in IC Design | 3 | 0 | 0 | 3 |
| 19CU3709 | Network Processors | 3 | 0 | 0 | 3 |

**19VL3706 SCRIPTING LANGUAGES FOR VLSI L T P C 3 0 0 3**

**Course Objectives : The students should be made to:**

1. Study scripting languages
2. Understand security issues
3. Learn concept of TCL phenomena

**Course Outcomes:**

**At the end of this course, the students should be able to:**

1. Explain advanced TCL
2. Discuss TK and Java script

**UNIT I INTRODUCTION TO SCRIPTING AND PERL 9**

Characteristics of scripting languages, Introduction to PERL, Names and values, Variables and assignment, Scalar expressions, Control structures, Built-in functions, Collections of Data, Working with arrays, Lists and hashes, Simple input and output, Strings, Patterns and regular expressions, Subroutines, Scripts with arguments.

**UNIT II ADVANCED PERL 9**

Finer points of Looping, Subroutines, Using Pack and Unpack, Working with files, Navigating the file system, Type globs, Eval, References, Data structures, Packages, Libraries and modules, Objects, Objects and modules in action, Tied variables, Interfacing to the operating systems, Security issues.

**UNIT III TCL 9**

The TCL phenomena, Philosophy, Structure, Syntax, Parser, Variables and data in TCL, Control flow, Data structures, Simple input/output, Procedures, Working with Strings, Patterns, Files and Pipes, Example code.

**UNIT IV ADVANCED TCL 9**

The eval, source, exec and up-level commands, Libraries and packages, Namespaces, Trapping errors, Event-driven programs, Making applications 'Internet-aware', 'Nuts-and-bolts' internet programming, Security issues, running un trusted code, The C interface.

**UNIT V TK AND JAVA SCRIPT 9**

Visual tool kits, Fundamental concepts of TK, TK by example, Events and bindings, Geometry managers, PERL-TK. JavaScript – Object models, Design Philosophy, Versions of JavaScript, The Java Script core language, Basic concepts of Python. Object Oriented Programming Concepts (Qualitative Concepts Only): Objects, Classes, Encapsulation, Data Hierarchy.

**TOTAL: 45 PERIODS**

**REFERENCES:**

1. Brent Welch,"Practical Programming in Tcl and Tk",Fourth Edition, 2003.
2. David Barron, "The World of Scripting Languages", Wiley Publications, 2000.
3. Guido van Rossum, and Fred L. Drake ", Python Tutorial, Jr., editor, Release 2.6.4
4. Randal L. Schwartz, "Learning PERL", Sixth Edition, O‟Reilly.

**19VL3707 HARDWARE AND SOFTWARE CO DESIGN L T P C 3 0 0 3**

**Course Objectives**

1. The students will learn various design steps starting from system specifications to hardware/software implementation and will experience process optimization while considering various design decisions.
2. Students will gain design experience with project/case studies using contemporary high level methods and tools.

**Course Outcomes**

1. To outline and apply design methodologies
2. To appreciate the fundamental building blocks of the using hardware and software co design and related implementation and testing environments and techniques and their inter-relationships
3. To modern hardware/software tools for building prototypes
4. To demonstrate practical competence in these areas.
5. Analyze various verification methods

**UNIT I SYSTEM SPECIFICATION AND MODELLING 9**

Embedded Systems , Hardware/Software Co-Design , Co-Design for System Specification and Modelling , Co-Design for Heterogeneous Implementation - Processor Synthesis , Single Processor

Architectures with one ASIC, Single-Processor Architectures with many ASICs, Multi Processor Architectures , Comparison of Co-Design Approaches , Models of Computation ,Requirements for Embedded System Specification .

**UNIT II HARDWARE/SOFTWARE PARTITIONING 9**

The Hardware/Software Partitioning Problem, Hardware-Software Cost Estimation, Generation of the Partitioning Graph, Formulation of the HW/SW Partitioning Problem, Optimization, HW/SW Partitioning based on Heuristic Scheduling, HW/SW Partitioning based on Genetic Algorithms.

**UNIT III HARDWARE/SOFTWARE CO-SYNTHESIS 9**

The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Distributed System Co-Synthesis

**UNIT IV PROTOTYPING AND EMULATION 9**

Introduction, Prototyping and Emulation Techniques, Prototyping and Emulation Environments, Future Developments in Emulation and Prototyping ,Target Architecture- Architecture Specialization Techniques, System Communication Infrastructure, Target Architectures and Application System Classes, Architectures for Control-Dominated Systems, Architectures for Data Dominated Systems, Mixed Systems and Less Specialized Systems

**UNIT V DESIGN SPECIFICATION AND VERIFICATION 9**

Concurrency, Coordinating Concurrent Computations, Interfacing Components, Verification, Languages for System-Level Specification and Design System-Level Specification, Design Representation for System Level Synthesis, System Level Specification Languages, Heterogeneous Specification and Multi-Language Co-simulation

**TOTAL : 45 PERIODS**

**REFERENCES:**

1. Ralf Niemann , “Hardware/Software Co-Design for Data Flow Dominated Embedded Systems”, Kluwer Academic Pub, 1998.

2. Jorgen Staunstrup , Wayne Wolf ,”Hardware/Software Co-Design: Principles and Practice” , Kluwer Academic Pub,1997.

3. Giovanni De Micheli , Rolf Ernst Morgon,” Reading in Hardware/Software Co-Design “ Kaufmann Publishers,2001.

**19VL3708 SELECTED TOPICS IN IC DESIGN L T P C 3 0 0 3**

**Course Objectives:**

1. This course deals with the supply circuit modules which are crucial modules in an IC design. Clock generation circuits play a major role in High Speed Broad Band Communication circuits, High Speed I/O‟s, Memory modules and Data Conversion Circuits.

2. This course focuses on the design aspect of Clock Generation circuits and their design constraints.

**Course Outcomes:**

- This course provides the essential know how to a designer to construct Supply reference circuits and Clock Generation Circuits for given design specifications and aids the designer to understand the design specifications related to Supply and Clock Generation Circuits.

**UNIT I VOLTAGE AND CURRENT REFERENCES 9**

Current Mirrors, Self Biased Current Reference, startup circuits, VBE based Current Reference, VT Based Current Reference, Band Gap Reference , Supply Independent Biasing, Temperature Independent Biasing, PTAT Current Generation, Constant Gm Biasing

**UNIT II LOW DROP OUT REGULATORS 9**

Analog Building Blocks, Negative Feedback, AC Design, Noise and Noise Reduction Techniques, Stability, LDO Efficiency, LDO Current Source, LDO Current Source Using Opamp.

**UNIT III OSCILLATOR FUNDAMENTALS 9**

General considerations, Ring oscillators, LC oscillators, Colpitts Oscillator, Jitter and Phase noise in Ring Oscillators, Impulse Sensitivity Function for Ring Oscillators, Phase Noise in Differential LC Oscillators.

**UNIT IV PHASE LOCK LOOPS 9**

PLL Fundamental, PLL stability, Noise Performance, Charge-Pump PLL Topology, CPPLL Building blocks, Jitter and Phase Noise performance.

**UNIT V CLOCK AND DATA RECOVERY 9**

CDR Architectures, Tias and Limiters, CMOS Interface, Linear Half Rate CMOS CDR Circuits, Wide capture Range CDR Circuits.

**Total: 45 Periods**

**References:**

1. BehzadRazavi, “Design of Integrated circuits for Optical Communications”, McGraw Hill, 2003.

2. Floyd M. Gardner ,”Phase LocK Techniques” John wiley& Sons, Inc 2005.

3. Gabriel.A. Rincon-Mora, "Voltage references from diode to precision higher order bandgapcircuits”,Johnwiley& Sons, Inc 2002.

4. High Speed Clock and Data Recovery, High-performance Amplifiers Power Management “ springer, 2008.

**19CU3709 NETWORK PROCESSORS L T P C 3 0 0 3**

Course Objectives

- Learn network processors
- Study commercial network processors
- Understand network processor architecture

Course Outcomes

Discuss network processor architecture

1. Compare different programming
2. Explain IOS technologies

**UNIT I INTRODUCTION 9**

Traditional protocol processing Systems – Network processing Hardware – Basic Packet Processing Algorithms and data Structures - Packet processing functions – Protocol Software – Hardware Architectures for Protocol processing – Classification and Forwarding – Switching Fabrics

**UNIT II NETWORK PROCESSOR TECHNOLOGY 9**

Network Processors: Motivation and purpose - Complexity of Network Processor Design – Network Processor Architectures architectural variety, architectural characteristics Peripheral Chips supporting Network Processors: Storage processors, Classification Processors, Search Engines, Switch Fabrics, Traffic Managers.

**UNIT III COMMERCIAL NETWORK PROCESSORS** 9

Multi-Chip Pipeline, Augmented RISC processor, Embedded Processor plus Coprocessors, Pipelilne of Flomogeneous processors. Configurable Instruction set processors – Pipeline of Electrogeneous processors – Extensive and Diverse processors – Flexible RISC plus Coprocessors – Scalability issues – Design Tradeoffs and consequences

**UNIT IV NETWORK PROCESSOR: ARCHITECTURE AND PROGRAMMING 9**

Architecture: Intel Network Processor: Multi headed Architecture Overview – Features- Embedded EISC processor - Packet Processor Hardware – Memory interfaces – System and Control Interface Components – Bus Interface. Programming Software Development Kit-IXP Instruction set – register formats – Micro Engine Programming – Intra thread and Inter-thread communication– thread synchronization – developing sample applications – control plane – ARM programming

**UNIT V IOS TECHNOLOGIES 9**

CISCO COS – Connectivity and scalability – high availability – IP routing – IP services – IPV6 – Mobile IP – MPLS – IP Multicast 0 Manageability – QoS – Security – Switching – Layer VPN2

**References**

1. Douglas E.Comer “Networks Systems Design using Network Processors” Prentice Hall JaN. 2003

2. Erik, J.Johnson and Aaron R.Kunze, "IXP2400/2806 Programming: The Microengine Coding Grade" Intel Press.
3. Hill Carlson, "Intel Internet Exchange Architecture & Applications a Practical Guide to Intel‟s network Processors" Intel press. www.cisco.com
4. Panas C. Lekkas, "Network Processors: Architectgures, Protocols and Paradigms Telecom Engineering)", McGraw Hill, Professional, 2003.
5. Patrick Crowley, M aEranklin, H. Hadminglu, PZ Onfryk, "Network Processor Design, Issues and Practices Vol-1" Morgan Kaufman, 2002.
6. Patrick Crowley, M a Frankliln, H. Hadimioglyum PZ Onufryk, Network Processor Design, Issues and Prentices vol.II, Morgan Kaufman, 2003.
7. Ran Giladi, Network Processors: Architecture, Programming, and Implementation, Morgan Kauffmann, 2008.